

GEIA CMC 4Q06 MEETING MINUTES

Dates: December 14 - 15, 2006

Place: San Francisco, CA USA

Note: Details of information presented are not provided here; the presentations are posted on the CMC web site.

December 14, 2006

Opening – Joe Watts (IBM)

Joe Watts opened the meeting setting an expectation that there would be at least 37 members in 2007.

The council agreed to these 2007 Meeting Places:

1Q07: Following ICMTS, Tokyo, Japan March 19-22

CMC meeting will be on Friday March 23

2Q07: Following the WCM, Santa Clara May 20-24

3Q07: Following BCTM in Boston in October

4Q07: Following IEDM in Washington, DC in December

Additional meeting details to be published.

MEXTRAM - Joachim Burghertz and Slobodan Mijalkovic (TUDelft)

Slobodan Mijalkovic will be leaving TUDelft. A replacement will be hired to take over MEXTRAM support. Updates on MEXTRAM were presented.

PSP – Gennady Gildenblat (ASU)

A list of requested PSP enhancements were overviewed.

Action Item:

Paul Humphries (ADI) will redo the CJSWG VGS measurement experiment performed by NXP and Maxim.

The council made the decision to release PSP102.2 in Verilog-A containing these updates:

1. WPE
2. dielectric constant
3. DELTVTO and FACTU0
4. removal of archaic syntax
5. NF support
6. separate parameters for source/drain junctions

The beta version release of PSP102.2 is targeted for ~3Q07.

It was reported that PSP SOI-PD is being tested by CMC companies as it is being developed.

Presentations were given by several members on circuit simulation speed and convergence with PSP. Ivan Pesic of Simucad showed PSP had trouble converging on some circuits. Infineon showed PSP was slower than BSIM4. William Liu of Maxim showed PSP is ~50% slower than BSIM4. Dick Klaassen of NXP showed PSP/BSIM4 speed ratio was between 1 to 2 depending on the simulator used.

Colin McAndrew showed PSP model evaluation time can be reduced by improving ADMS which generates the model code. A 20-25% speed up in model evaluation time is expected. The speed-up comes from improved efficiency of the derivative code.

Jim Victory (Jazz) presented feedback on PSP from three of his customers. There was satisfaction with IP3 simulation accuracy; although simulation time was ~2x that of BSIM3, there were no convergence problems. On Friday Synopsys reported they received reports of customers having convergence problems using the NQS form of the model.

Action Item:

Colin McAndrew will provide a date for the ADMS update with improvements for model evaluation time.

Action Item:

Colin McAndrew will redo his PSP runtime analysis using a larger number of transistors.

Action Item:

Ivan Pesic will make the model parameter sets used in his model speed/convergence analysis available to other CMC members.

Action Item:

Ivan Pesic will report more details on his model speed/convergence analysis, e.g., iteration count.

Ivan made the motion for the council to reconsider making HiSIM a standard..

The council decided to entertain further HiSIM evaluation results at 1Q07 meeting, provided this work does not interfere with planned PSP improvements.

The evaluation is to include:

1. Simulations with a simulator other than Smartspice.
2. Financial impact on CMC budget if HiSIM were to be adopted by CMC.
3. Why PSP failed in Ivan's simulations
4. Million transistor circuit results if available

Colin McAndrew assembled a detailed list of requested PSP improvements with priorities. Improving simulation time and developing non-uniform lateral and vertical doping models are the highest priority. The doping models were identified as a long-term research project.

The council made the decision to implement the distinct source and drain diode parameters in PSP with name nomenclature like BSIM4 – this will mean parameter sets for the new model would be backward incompatible.

Members were reminded that requests for improvements need to be supported with data and information about the test structures.

Gert-Jan Smit of NXP gave a presentation on the development of the PSP-based FINFET model.

LDMOS Model Presentations:

Three developers gave overviews of their LDMOS models: Adrian Ionescu (HV-EKV), Dick Klaassen (MM20), and Masataka Miyake (HiSIM-LDMOS). There will be updates to HV-EKV and MM20 at the end of March. There will be an updated version of HiSIM-LDMOS available at the end of December 2006.

Model evaluations were presented by Jazz Semiconductor, Intersil, and National Semiconductor.

Yutao Ma reviewed the roadmap for selecting an LDMOS model standard. Additional evaluations of these three models will be presented at the 1Q07 and 2Q07 meetings. Selection of the standard model is targeted to following the 2Q07 meeting. Note, the model selected might require updates prior to initial release of the standard version.

Joe Watts closed the December 14 meeting.

December 15, 2006

Subcommittee Reports

Resistor Model Subcommittee – Colin McAndrew (Freescale)

Members are asked to evaluate r3_cmc prior to the 1Q07 meeting. The CMC will vote on standardization of this model at the 1Q07 meeting in Tokyo.

MOS Varactor Model Subcommittee – Jim Victory (Jazz Semiconductor)

A “beta” model was sent out on December 5, 2006 for member testing. The subcommittee is targeting June 2007 for completion of the “rev1” model with improvements. The model will be delivered in Verilog-a only. Members will be expected to evaluate the model in preparation for a standardization vote that is targeted for the 3Q07 meeting.

QA and Release Subcommittee – Rob Jones (IBM)

V1.2 of the QA test suite and documentation are on the CMC website. Members are asked to evaluate this. The subcommittee is targeting baseline level of QA test capability for all six CMC models (BSIM3, BSIM4, BSIMSOI, PSP, MEXTRAM, and HiCUM).

Rob Jones started a spreadsheet for tracking change and release activities on each of the standard models.

Model Interface Subcommittee –

Geoffrey Coram proposes that this group suspend operation until the Verilog-A committee completes its work on statistical parameters for the Paramset. He estimates that this will be the second half of 2007.

The CMC declined Geoffrey’s proposal and asks that this subcommittee continue efforts working with the Verilog-a committee and working on the objective and value of this project. The CMC would like the subcommittee to more specifically define the scope of capabilities the interfaced will provide. In addition the CMC noted that this initiative will require additional work from EDA vendors and they need to see some potential value to support the new standard.

Action Item:

Joe Watts will work with Geoffrey on how the subcommittee should proceed.

Well Proximity Effects Subcommittee – Mark Basel (Mentor)

Subcommittee plans to bring engineered stress effects into their efforts. Subcommittee generated some FAQs to go out as press releases.

Action Item:

Joe Watts will follow up with the GEIA to issue the WPE FAQs as press releases.

Parasitic Extraction Subcommittee – Mark Basel (Mentor)

Subcommittee intends to generate guidelines on parasitic extraction that include the recommended boundaries between device and interconnect parasitics. Subcommittee is targeting a first pass of the guidelines by the 1Q07 meeting for members to review.

Implementation of Models in EDA Tools

Vendor members presented summaries of the versions of models implemented in their tools.

Action Item:

Weidong Liu of Synopsys will share with the PSP team convergence problems experienced with the NQS model.

Website Update – Keith Green (TI)

The GEIA expects to roll out new website functionality in early 2007.

Action Item:

Keith Green will set up a phone call with Chris Denham and CMC officers to review strategy for new website functionality roll-out.

Verilog-A Test Suite – Marek M. (Tiburon)

Final release will be posted on the CMC website.

Budget Discussion – Robert Lomenick (Intersil)

A surplus of \$62K in 2006 is expected. The council approved this usage of the surplus:

MOS Var Support 2005	\$25K
MOS Var Support 2006	\$25K
HiCUM Support	~\$6K – half of remainder
Mextram Support	~\$6K – half of remainder

Joe reported that he had received a suggestion to support fund HICUM Level 0 as a standard as well as HICUM Level 2. This received no other support by the CMC and the 2007 proposed budget was reviewed and approved by the council.

BSIM Models – Chenming Hu and Chung-Hsun Lin (UC-Berkeley)

Morgan Yang was introduced as the new post-doc responsible for BSIM model support.

BSIM4.6.0 was released on 12/13/2006.

BSIM4SOI4.1 beta release is targeted for end of December 2006. The model includes some improvements and bug fixes.

BSIMMG1.0 alpha version was released in October 2006 in Verilog-a. An overview of the model was presented. An asymmetric independent gate model will be released in early 2007.

Action Item:

The BSIM team will team update model documentation (manual) with more details on how NF is implemented.

HiCUM – Jim Victory (Jazz Semiconductor)

A slide from Michael Schroter described a new Version 2.23 of HiCUM. The council decided it wants Michael to hold off the release of 2.23 and address its concern about inconsistency between the ac and transient models and that the Verilog-A implementation of the model be the complete definition of the model. A member reported that the model documentation specifies some delays which are not include the Verilog-A should be added in the C-implementation. Also they want him to follow the council's QA and Release procedures.

Action Item:

Jim Victory will communicate to Michael Schroter that the council asks that he hold off the release of version 2.23 of HiCUM and address council's concern about inconsistency between the ac and transient models and that the release follow the council's QA and Release procedures. Also he should make the Verilog-a model a complete representation.

Agilent HBT Model Overview - Masaya Iwamoto (Agilent)

Members interested in evaluating this model should contact Masaya Iwamoto.

Only two members expressed an interest in standardizing an HBT model.

Goals for 2007 – All

The council assembled a draft list of goals for 2007. The list will be circulated to members for ranking then finalized at the 1Q07 meeting.

Action Items Carried Over From Previous Meeting –

Action Item: TI will provide data to TU Delft on the Ibc diode currents, and NXP and TU Delft will investigate further the need for this and the physical formulation; the tunneling current will be included in the next beta release.

Action Item: Officers will develop an orientation plan for new members.

Action Item: Joe will update the names policy based on the discussion at the meeting. It will be posted on the CMC website and announced via a GEIA press release.

Next Meeting Planning – All

1Q07 Meeting will be held on March 23. This is an opportunity to recruit more Japanese companies into the CMC. The meeting agenda may include

1. Provide an introduction to the CMC for guest attendees from Japanese companies.
2. EDA Vendor Inputs on simulation strategy for large circuits and how model speed plays into this.
3. Tutorial on simulations of large circuits by an expert, e.g., Ken Kundart
4. LDMOS Model Evaluations
5. Finalization of 2007 Goals
6. Vote on R3_CMC standardization
7. 2007 Budget

Joe Watts closed the December 15 meeting.

Attendees

Last Name	First Name
Moinian	Shahriar
Poore	Rick
Iwamoto	Masaya
Croston	Robin
Topalogu	Rasit
Humphries	Paul
Tolikas	Mary
Mertens	Samuel
Lee	Mankoo
Ito	Akira
Ma	Yutao
Xie	Jushan
Bhardwaj	Sunil
Takada	Yorio
Kosukegawa	Tsutomu
Ito	Makoto
McAndrew	Colin
Jallepalli	Srinivas
Watts	Josef
Jones	Rob
Mudanai	Sivakumar
Lomenick	Robert
Cherne	Richard
Victory	James
Mansour	Nabil
Liu	William
Basel	Mark
Smith	Linda
Szabo	Andras
Francis	Pascale
Iizuka	Takahiro
Klaassen	Dirk
Huizing	Bert
Smit	Gert-Jan
Onozawa	Kazunori
Resvani	Ali
Park	Jin-Kyu
Pesic	Ivan
Shaw	Colin
Ino	Yoshihisa
Hiroshi	Koike

Furui	Yoshiharu
Charbuillet	Clerment
Liu	Weidong
Green	Keith
Tatsuya	Ohguro
Shapira	Shye
Liu	Sally
Wan	Daniel
Gildenblat	Gennady
Mijalkovic	Slobodan
Burghartz	Achim
Dunga	Mohan
Lin	Chung-Hsun
Hu	Chenming
Ionescu	Adrian
Muira-	
Mattausch	Mitiko
Mattausch	Hans Juergen
Miyake	Masataka
Chen	Wanqiang
Yamamoto	Tsuyoshi

Companies with **ACTIVE** voting status:

Agere Systems
Agilent Technologies
Analog Devices
Ansoft Corporation
Atmel
Broadcom
Cadence Design Systems
Cypress Semiconductor
Elpida
Evolvable Systems Research
Institute
Freescale Semiconductor
IBM
Infineon
Intel
Intersil
Jazz Semiconductor
Maxim
Mentor Graphics
National Semiconductor
NEC Electronics
NXP
Renesas Technology Corporation
RF Micro Devices
Simucad

Companies with **INACTIVE** voting status:

Sony
STARC
ST Microelectronics
Synopsys, Inc
Texas Instruments
Toshiba Corporation
Tower
TSMC
United Microelectronics Corporation

AMD
LSI
Samsung
Sandia National Laboratories
SRC
Xpedion