

Minutes of CMC Telecon: November 10, 2004

Attendees: Renesas, TU-Crete, IBM, TI, Freescale, Infineon, Silvaco, Philips, Penn State University, UC-Berkeley, Agere, Hiroshima University

Colin McAndrew (Freescale) reported on the selection of transistor geometries from the IBM 90nm data to be used in the evaluation of the DC I-V equations of the next generation standard MOSFET model candidates:

Length arrays will be those transistors with $W=0.12\mu\text{m}$ and $10\mu\text{m}$; width arrays will be those transistors with $L=0.08\mu\text{m}$ and $2\mu\text{m}$ for both NMOS and PMOS (total of 24). Reports with overlays of I-V sweeps will be required for the four corner devices and $W/L=2/.24$, $0.24/0.08$ (NMOS), and $0.3/0.08$ (PMOS). Overlays of parametric characteristics will be required for all transistors of the four arrays.

It was noted that data is missing for PMOS $W/L=0.12/10$ and a range of the NMOS sizes is missing -55C data.

Action Item:

Joe will check on the missing data.

Action Item:

Colin will send out a summary of sizes to be used in the model evaluations as well as data trend plots. Keith will post these on the CMC website. (DONE)

Action Item:

Colin will assess the non-common pad DUT DC I-V data.

Action Item:

Colin will take lead on following up with the sub-team to assess the capacitance data.

Meeting adjourned.

This meeting was conducted in accordance with the EIA Legal Guides and EIA Manual of Organization and Procedure.