CMC Teleconference: October 20, 2004

Attendees:

Freescale, IBM, TI, TU-Crete, Penn State University, Silvaco, Renesas, Agere, NEC, Philips, Nassda, UC-Berkeley, ADI, Intel, Infineon, Intersil, UMC

Topic of discussion was the IBM 90nm test data for next generation MOSFET model evaluation and requirements for testing

Peter Lee's (Renesas) comments on data:

For extrapolated VT v. L, he did not notice any VT rolloff, just VT roll up. Joe reported that data is provided for shortest devices, so no additional data can be provided.
Peter observed there are two sets of I-V data: one with common source and gate pads and one with separate pads. Data is not taken to as low of voltage on devices with separate pads.

Action Item: Joe to take data to lower voltages on devices with separate pads. 0.05V (DONE)

Michael Ridinger (Silvaco) observed drain current values do not agree between VDS and VGS sweeps. Michael will send Joe specifics and he'll look into this. (DONE)

Michael also pointed out that the VT equation in item #11 of the testing requirements document (MHC_deleverables.doc).

Action Item: Michael to send Keith the correction and Keith will update the document. (DONE)

Colin McAndrew's (Freescale) observations:

There is a subset of devices for which all temperature data is available. Recommendation is to weed out some sizes: keep sizes that are part of width and length arrays.

Colin requests drawn lengths and widths of devices.

Action Item: Joe will provide drawn widths and lengths. (DONE)

Colin will organize consensus on which sizes to use for reporting model test. This will encompass data discrepancies found by him and Michael. (DONE)

NEC to identify for Joe data sets for which #fingers has not been normalized out. Joe will correct this and send Keith updated data for posting on website. (DONE)

Joe will provide effective TOX inv he has already taken. (DONE)

It was agreed we will used drawn W and L as our references in the model evaluation.

Action Item: Joe will identify the nominal gate length. (DONE)

Jane Xi (UCB) requests separate data sets for diode current.

Action Item: Joe will provide both forward and reverse from large junction capacitance structures. (DONE)

Joe reported that we not need to consider STI stress effect from length direction due to wide moat, though the effect cannot be discerned from the data.

There was concern about stress effect in RF DUTs. Joe pointed out that there are DC I-V data that may assist with this.

Jane pointed out CV data shows some non-idealities.

Action Item: Joe to review gate capacitance data. He will follow up on getting total gate capacitance data measured at the gate. (DONE for PFET, TBD for NFET))

Joe reported the the RF data is most reliable up to 50GHz, though perhaps usable up to 100GHz.

It was agreed we would teleconference again on 11/10/05 to review action items above.

Schedule for Phase II:

Target Feb. 18, 2005 for completion of model testing by sponsors.

Meet in Dallas in March to review test results.

Meeting adjourned.

This meeting was conducted in accordance with the EIA Legal Guides and EIA Manual of Organization and Procedure.