

# Minutes of Compact Model Council Meeting

## September 16, 2004 Face-to-Face Meeting in Montreal

### Companies and Universities in Attendance:

Infineon, Atmel, Intersil, Broadcom, Agilent, Nassda, Synopsys, IBM, WMC, TI, Freescale, TU-Delft, ST, Analog Devices, Silvaco, Philips, Cadence, UCSD/TU-Dresden

### 1. Membership Review (Joe Watts – IBM/Chair)

Joe reported that Tower Semiconductor may join CMC, increasing the membership total to 25.

### 2. Treasurer's Report and Budget & Dues for 2005 (Robert Lomenick – Intersil/Treasurer)

Robert reported the CMC will have a 2004 budget excess of approximately \$17,000. He noted this must be spent by year's end or GEIA will absorb it.

Joe led discussion on what to do with the budgetary excess. Funding a project to develop standard model regression testing capability was suggested and discussed. Concern was expressed over whether there would be sufficient funding for it. Another suggestion was to fund development of a reference Verilog-a solver, a project proposed by Geoffrey Corum in July. Lastly, the suggestion was made to fund development of a power MOSFET model. However, there was member concerned about diverting the CMC's focus from standardization to research. No decision was reached.

#### Action Item:

Officers will present a recommendation for spending this year's budget excess at the December meeting.

CMC members will approve a budget at the December meeting.

### 3. Chairman's Topics

Joe reported that the current CMC officers recommended keeping the same officers for another year, in part to help ensure continuity and closure on the next generation MOSFET standard project. Consensus in the meeting was to do this. It was also recommended that we hold elections every two years. There was a suggestion that we might stagger the elections of officers: two elected one year, two the next, in order to help with continuity of leadership.

Joe reviewed a document prepared by the officers outlining CMC member's responsibilities and benefits. This has been posted on the CMC website.

Joe requests all presentations be done electronically via the CMC's new DLP.

Joe addressed a request made for dial-in service to CMC's face-to-face meetings. The officers recommend against this, in part to encourage in-person attendance.

#### 4. Status of Implementations of Standard Models

Warren presented a summary of Synopsys HSPICE support. See presentation for details.

Michael Ridinger presented a summary of Silvaco support. See presentation for details.

Action Item:

Pei Yao (Cadence) will send Keith Green (TI/CMC Secretary) an update on Cadence tool support of standard models for the CMC's website; Cadence will also post this to [www.designers-guide.com](http://www.designers-guide.com)

#### 5. Bipolar Support

HiCUM Update (David Sheridan – IBM and Michael Schroter – TU-Dresden):

Michael reviewed simulator support for HiCUM. Cadence reports all bugs fixed. Contact them for latest version. Michael reported a planned release of v2.2 in Q404 in Verilog-a and a stand alone solver; DEVICE will be provided to cooperation partners only.

See Michael's presentation for additional details.

There was a question about the status of HiCUM-lite (level-0). This is still supported. Infineon requests implementation of level-0 in Spectre. Cadence will do this using the Verilog-a code.

Action Item:

Pei Yao will update CMC at December meeting on status of HiCUM's implementation in Spectre.

Mextram Update (Slobodan Mijalkovic – Delft and Paul Humphries – ADI):

There is a new Mextram Users Group (MUG) website: <http://hitec.ewi.tudelft.nl/mug/>  
The site contains code, documentation, announcements, etc.

MUG met on 9/15 and assembled a list of action items. See presentation for details. The group recommended that bugs and other announcements go to CMC members via Joe Watts who maintains the email list.

Action Item:

Keith Green will update CMC's standard model bug-fix procedure document and post it to the CMC website. The updates will state the following:

- Bugs found should be reported immediately to model developer.
- After verification, developer will post bug report on support website with either a proposed fix or notification that fix will be forthcoming if significant effort required.
- Developer will then request Joe Watts (IBM/Chair) notify CMC members of bug fix website update.

6. Resistor Model Update (Colin McAndrew – Freescale)

Colin reviewed the team's progress since last CMC meeting. It has begun evaluating models provided by members for two-terminal non-linear resistors using Verilog-a. Model invertability, e.g., providing resistance and calculating resistor length, is done using zero-bias resistance. See presentation for summary and action items from team's meeting on 9/15. #1 item is to do an apples-to-apples comparison of the three models provided and give an update on this at the December CMC meeting.

Expectation is to complete the two-terminal resistor model effort prior to tackling a three-terminal resistor model.

7. Power MOSFET Model Update (Keith Green – TI)

Philips will be adding self-heating to MOS Model 20 and releasing this in early 2005. Drain extension velocity saturation effect is tentatively on their list of improvements for 2005, but this depends on the needs of internal customers.

The decision was made to put this team in hibernation until new public domain models come available.

Dick Klaassen (Philips) is interested in having TI test the new model after/if they put velocity sat into the model.

8. Proximity Effect (Paul Humphries – ADI)

The team met on 9/15. See presentations for details.

Paul pointed out that there is already a path to solution: implement custom equations via subcircuit using whatever measures from layout extraction or via CDF. This approach does not rely on instance parameters, since the .model card can be parameterized in terms of layout information.

Another solution is to provide an instance-based approach, e.g.,  $\Delta V_{T0}$ , which is supported in some simulators. Yet another is to just use the current stress model for any of the arbitrary effects.

There was opinion that the CMC charter is not to develop equations for proximity effects for all sorts of layouts, especially the unusual cases.

TSMC reported they have a model they plan to present at the December CMC meeting.

#### 9. Verilog-a Update (Colin McAndrew - Freescale)

Colin provided an overview of updates to Verilog-a. See presentation for details. Updates have been finalized and submitted to the Accelera committee. Approval is pending. Proposed changes can be viewed at the website noted in presentation. Colin recommends members review these in detail. Colin reported there will be a Verilog-a tutorial by Geoffrey Corum (ADI) at BMAS on Oct. 21 and 22 in San Jose.

#### 10. BSIM3/4 Update (Jane Xi – UCB & Keith)

Action Item:

Jane Xi (UCB) will release the beta code for BSIM4.5.0 on 9/24 for testing.

Actions Item:

Members who requested changes are required to test their updates in BSIM4.5.0. These tests will be reviewed at the December meeting then the CMC will make a decision about the final release of BSIM4.5.0.

Action Item:

Keith will follow up with Jane about the CMC's decision at the 2Q04 meeting to update BSIM3 CAPMOD=3. Per action item from that meeting, UCB needs to produce beta code for evaluation.

#### 11. Next Generation MOSFET Model Update (Joe)

Action Item:

Joe Watts will send Keith Green the data for next generation standard MOSFET model evaluation by 9/24. Keith will post this to the CMC website and send out notification to CMC members.

Joe reviewed the list of member sponsors for each of the four remaining candidate models.

It was agreed to identify a sponsor team lead for each of the candidate models: Michael Ridinger for HiSIM; Colin McAndrew for PSP; Joe will contact Peter Lee

and Judy An to see if they'll coordinate the BSIM5 effort; as the sole sponsor for EKV Infineon will lead the EKV effort.

It was decided to put off the presentations on model evaluations from 4Q04 to 1Q05.

**Action Item:**

Joe Watts will call a teleconference for October to discuss the standard dataset. In that teleconference the CMC will pick a date for the 1Q05 meeting to review next generation standard MOSFET model evaluation results.

With regards to the standard dataset, Joe reported that DUTs of transistor widths less than 2um are multiples in parallel to minimize local effects. Gate and body pads are shared so it is not possible to ascertain certain leakages, e.g., gate to body tunneling. Joe will provide wiring capacitances and layout of s-parameter structures.

In ballots after the 1Q05 meeting, all member companies will get to vote for two models. The top two vote getters move forward. We will decide later how to address final selection.

## 12. Membership Matters (All)

There was membership concern expressed about the cost of GEIA overhead.

**Action Item:**

Officers will investigate GEIA overhead charges to develop an understanding of whether they are reasonable and whether the CMC is getting full utilization of GEIA resources.

## 13. Next Meeting planning (Joe Watts)

The 4Q04 meeting will follow IEDM in San Francisco, CA, and be held on December 17, 2004. The agenda will include current standard models update status, Next Generation MOSFET standard model process, standard resistor model update, Verilog-a update, 2005 meeting planning, and CMC goals for 2005.

Meeting Adjourned.

This meeting was conducted in accordance with the EIA Legal Guides and EIA Manual of Organization and Procedure.