

CJSWG's Gate Bias Dependence; after NXP's preliminary results

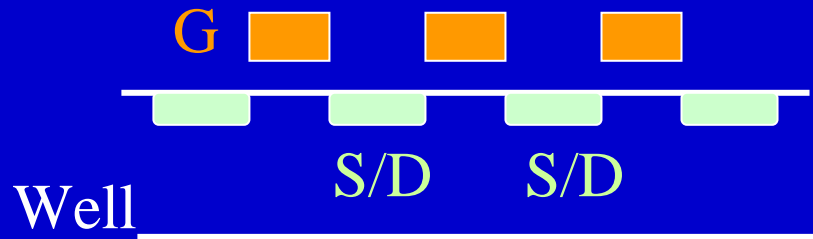
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Device Modeling
Maxim Integrated Products

Recap (yes, pun intended)

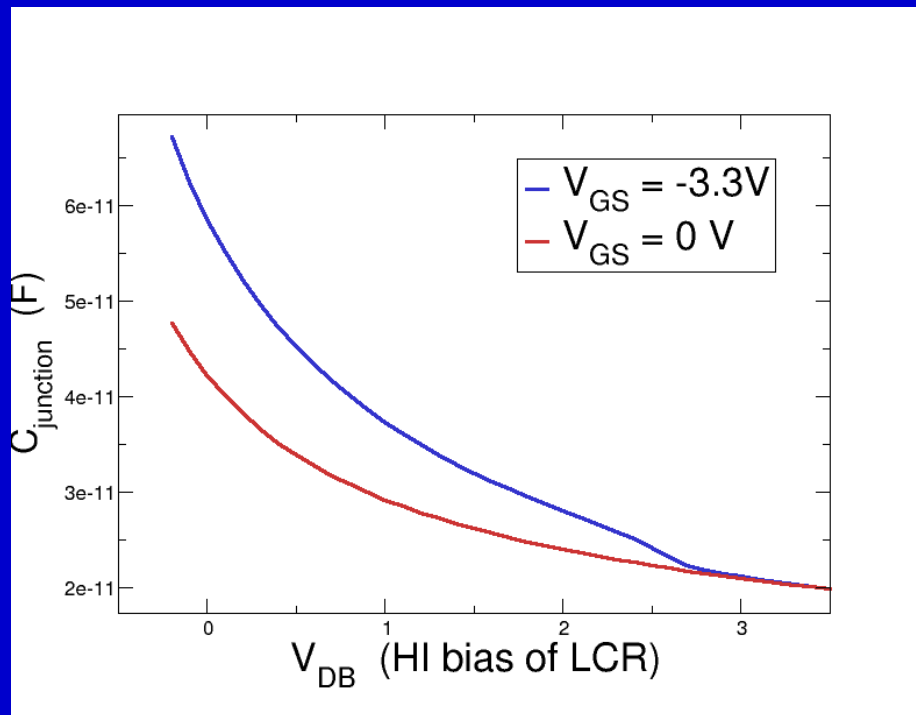
1) Maxim reported CJSWG as a function of VGS in 10/2006



Gate: Voltage Source

S/D: LO

Well: HI, $-3.5 \rightarrow 0.2$ V



100 kHz

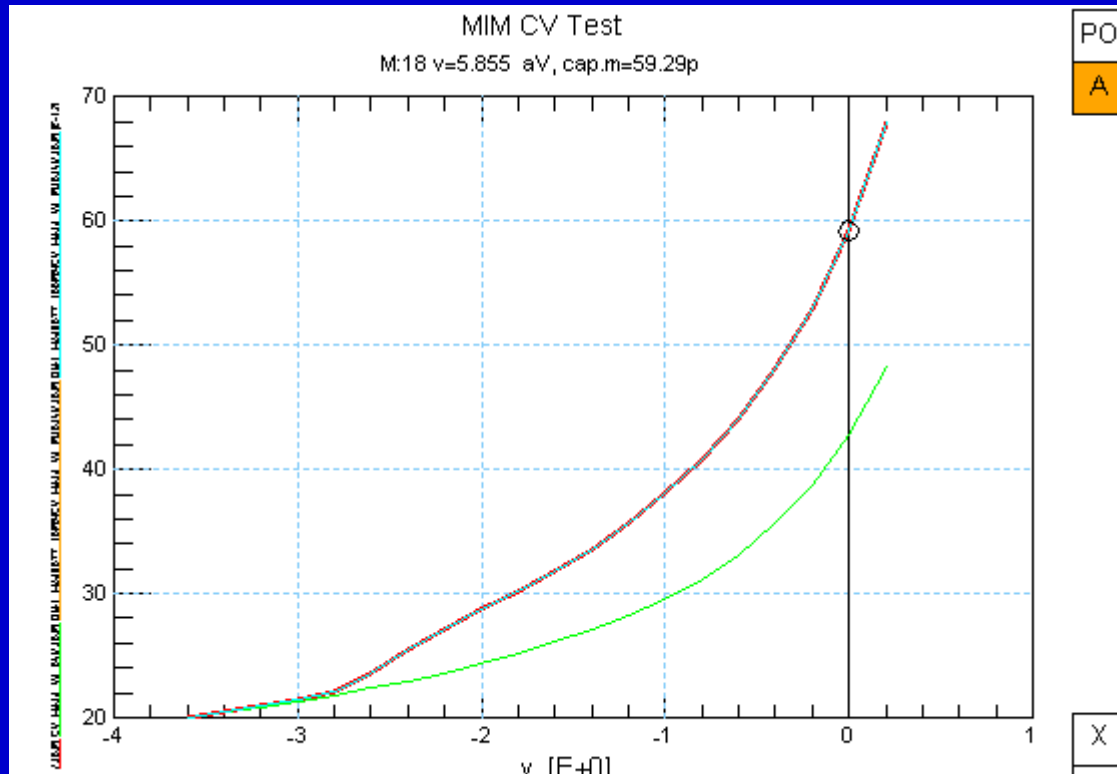
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2) NXP subsequently suggested 3 possibilities for CJSWG's "apparent" dependence on VGS

- Compliance dependence of the Vgs SMU
- LCR frequency dependence
- Phase Angle may deviate 90 deg

Remeasurement: Compliance Dependence

Compliance = 100uA, 10mA, 100 mA

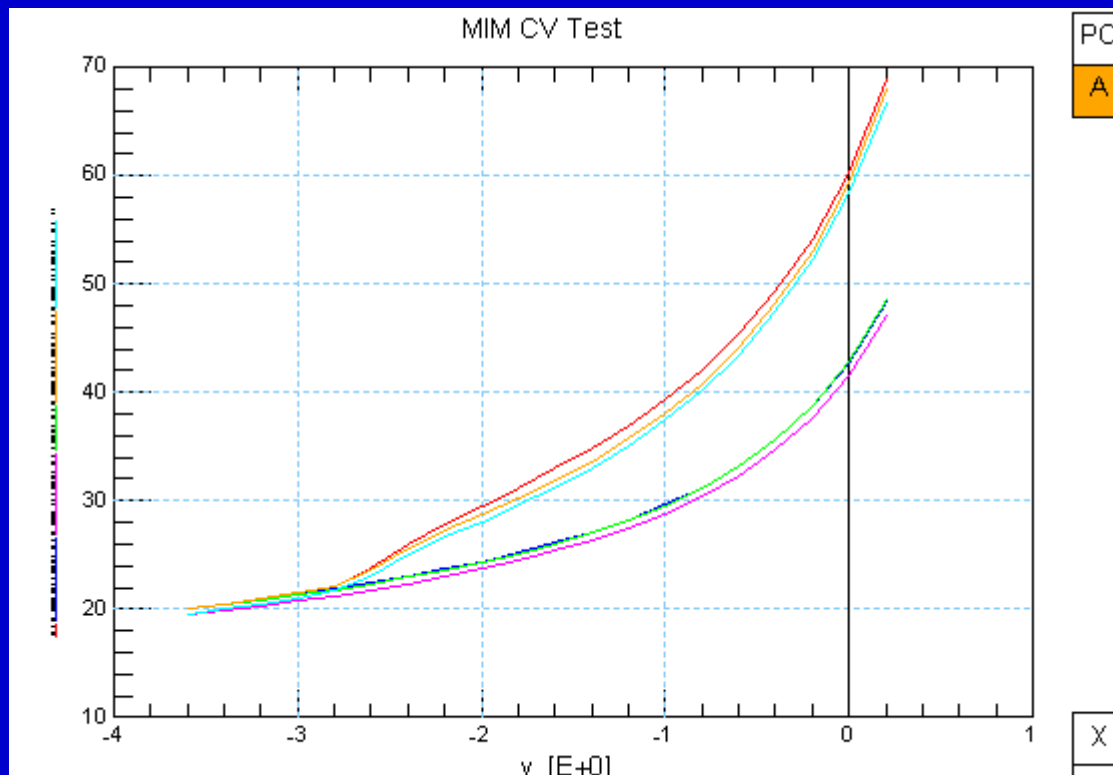


Maxim finds virtually no dependence on compliance.

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Remeasurement: Frequency Dependence

Frequency = 10 kHz, 100 kHz, 1 MHz

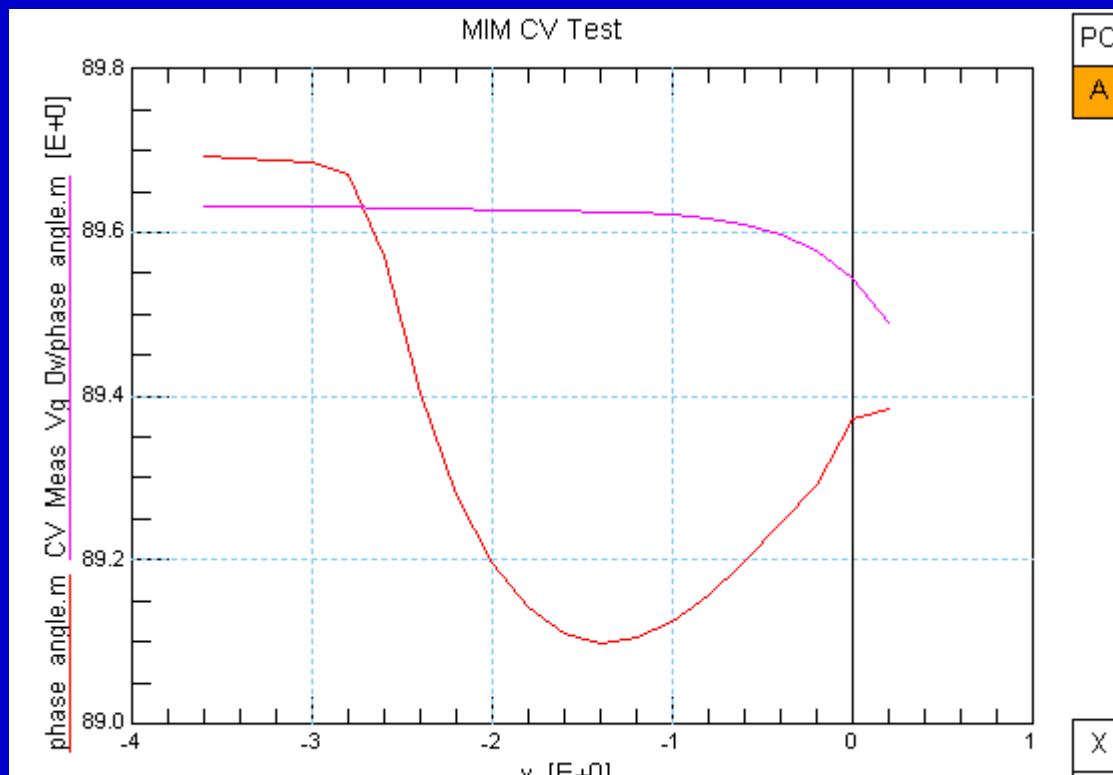


Some frequency dependence is observed at *both* VGS=0 and -3.3V. Frequency can't explain the 30% difference.

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Remeasurement: Phase Angle

Phase angles at $V_{gs} = 0$ and $-3.3V$



Indeed phase angle behavior is not smooth for the $-3.3V$ curve. However, they are both close to 90 degree.

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Summary

1. We still believe the CJSWG has strong VGS dependence.
2. In fact, knowing that our structure's CJSWG: CJ is 1.6 : 1, the 30 % overall junction capacitance increases means CJSWG increases by 50% as VGS changes from 0 to -3.3V.
3. There was no dependence on compliance.
4. The frequency dependence can't explain the 30% change.
5. The phase angles are close to 90 degree.