MOS Model 20

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*** NXP Research**

TU/e

technische universiteit eindhoven

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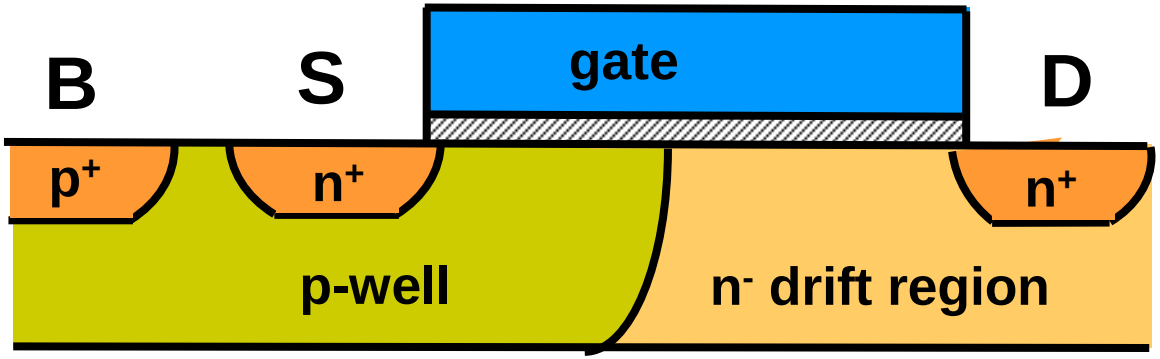
Contents

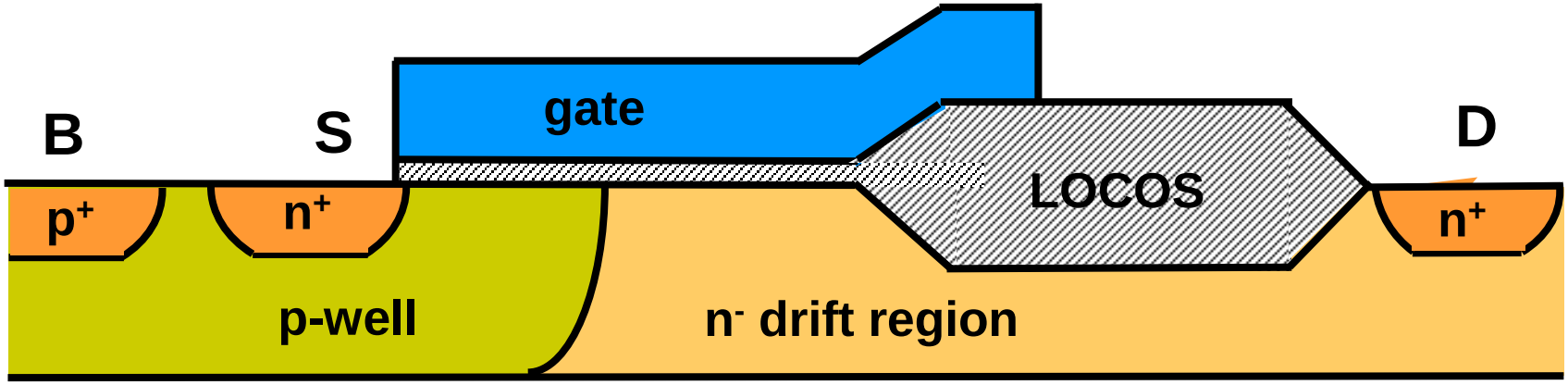
- introduction
- physics and features
- results
- versions, source code, documentation

Introduction: LDMOS devices

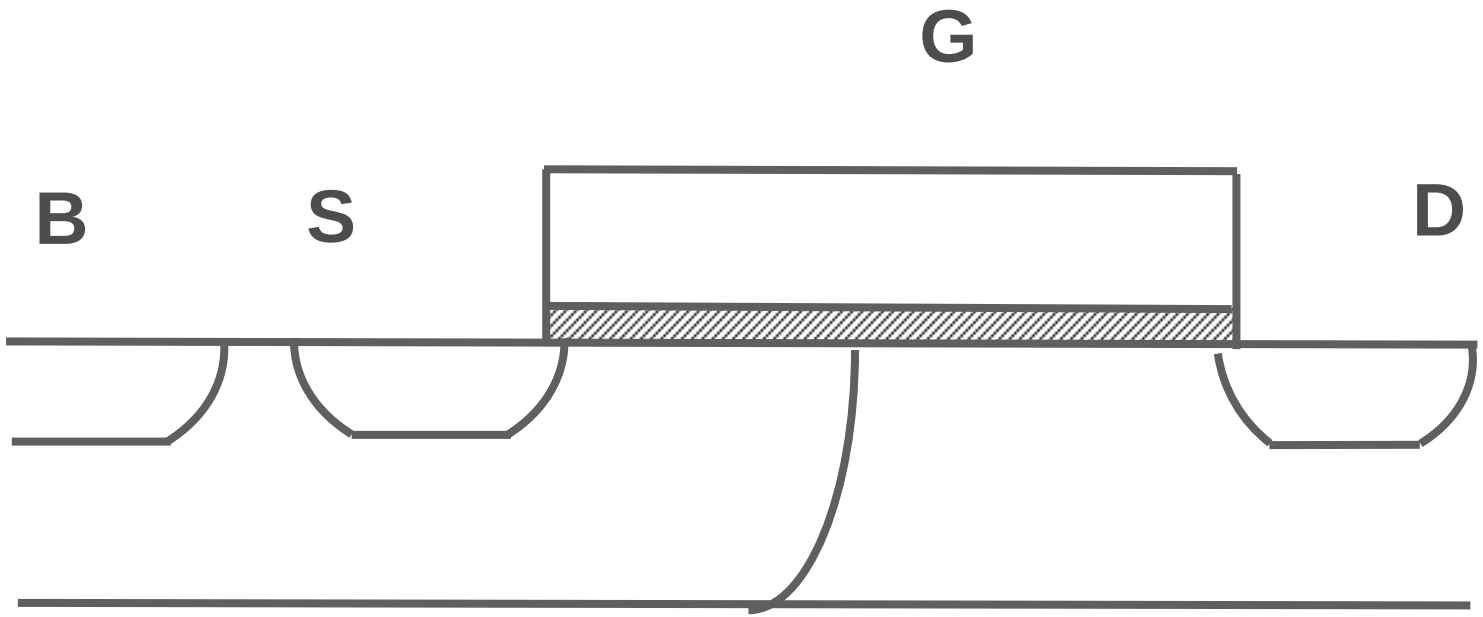
LV-LDMOS



HV-LDMOS



Introduction: LV-LDMOS Modeling



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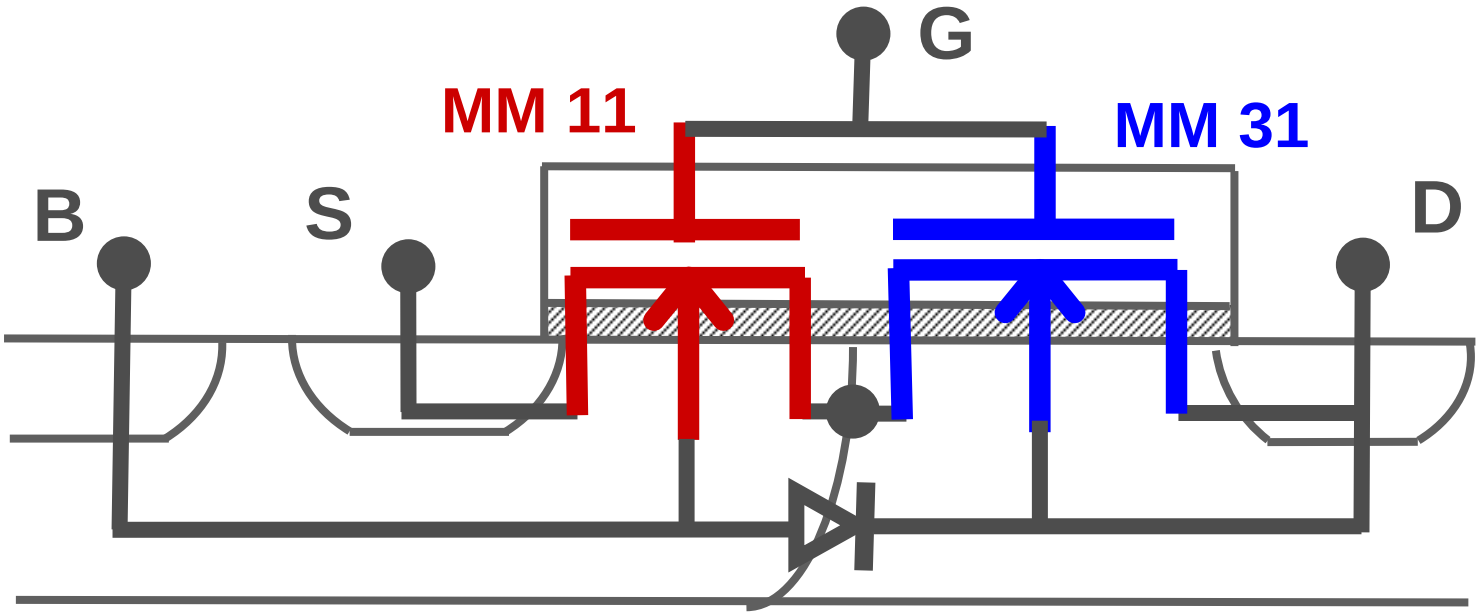
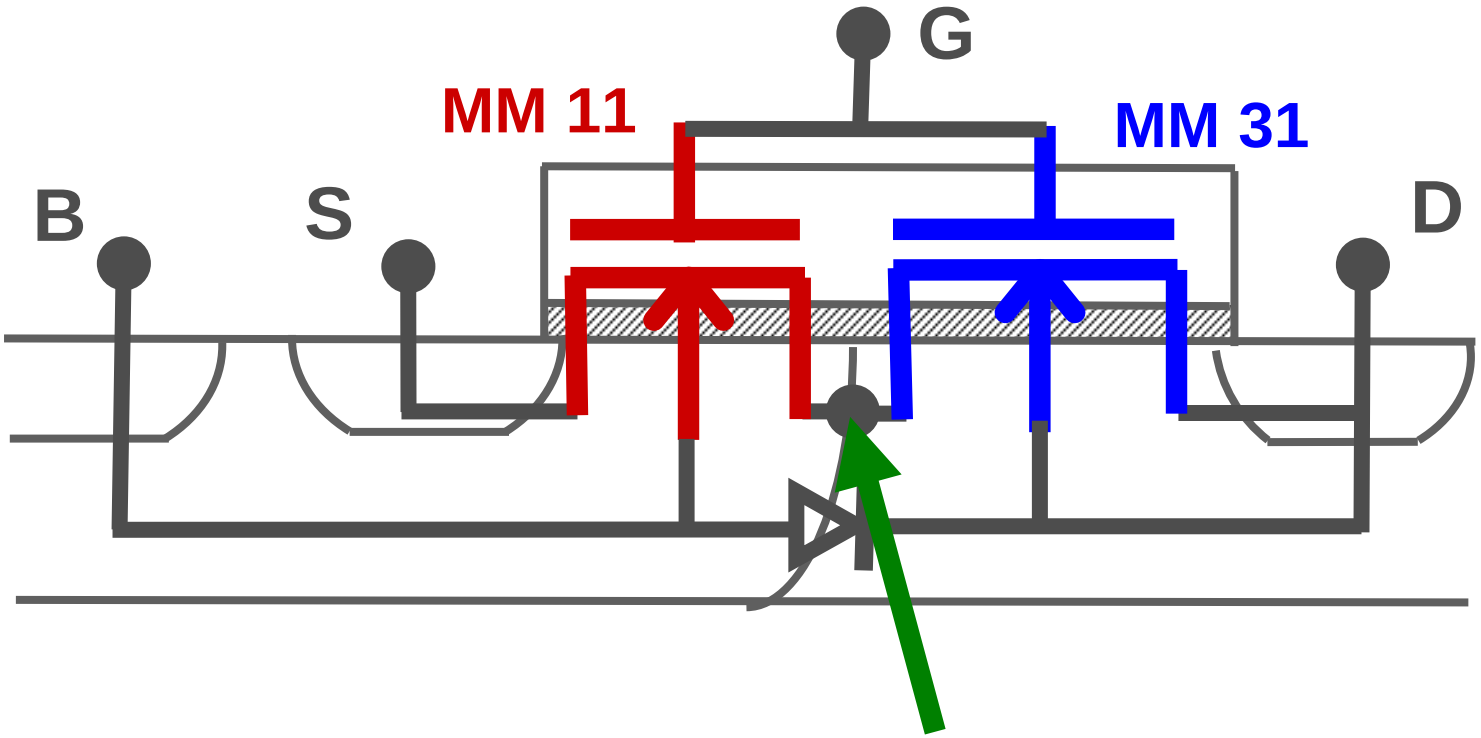


MM11: to model channel region, normal MOS device

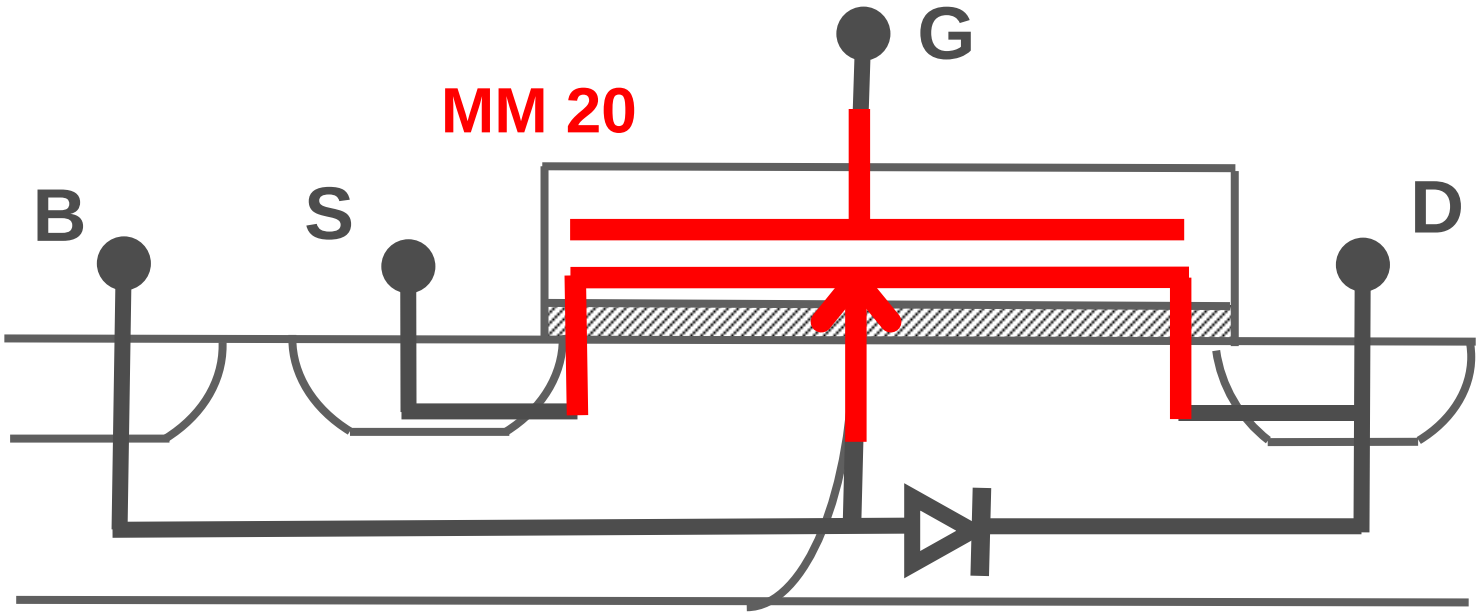
MM31: to model the extended drift region

Introduction: LV-LDMOS Modeling



Di: internal-drain node

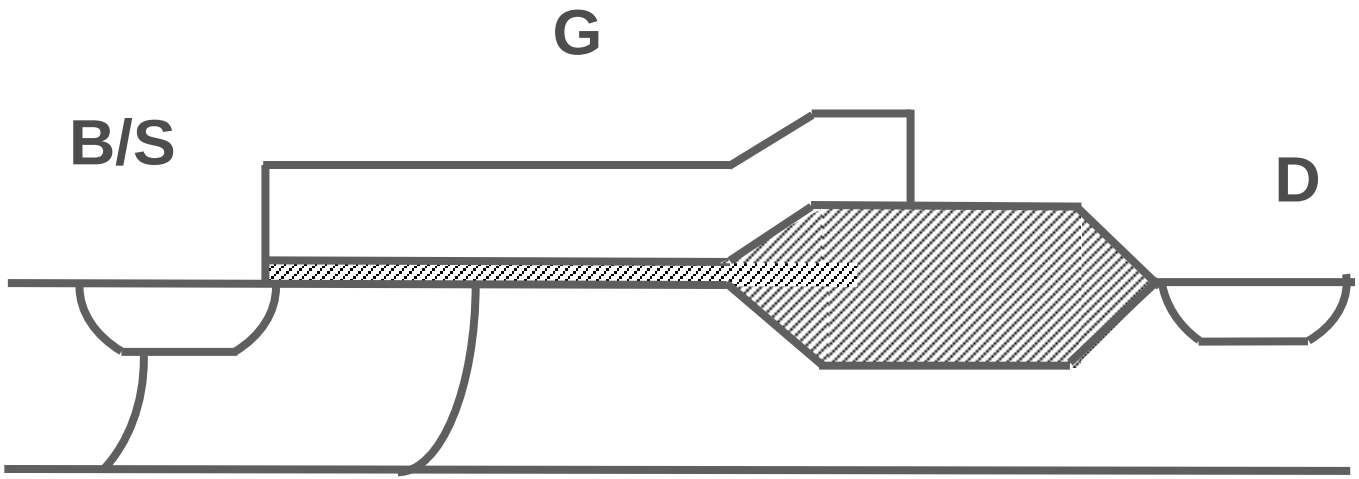
Introduction: LV-LDMOS Modeling



Di: calculated <u>inside</u> model

<u>advantage</u>: controlled voltage / convergence

Introduction: HV-LDMOS Modeling



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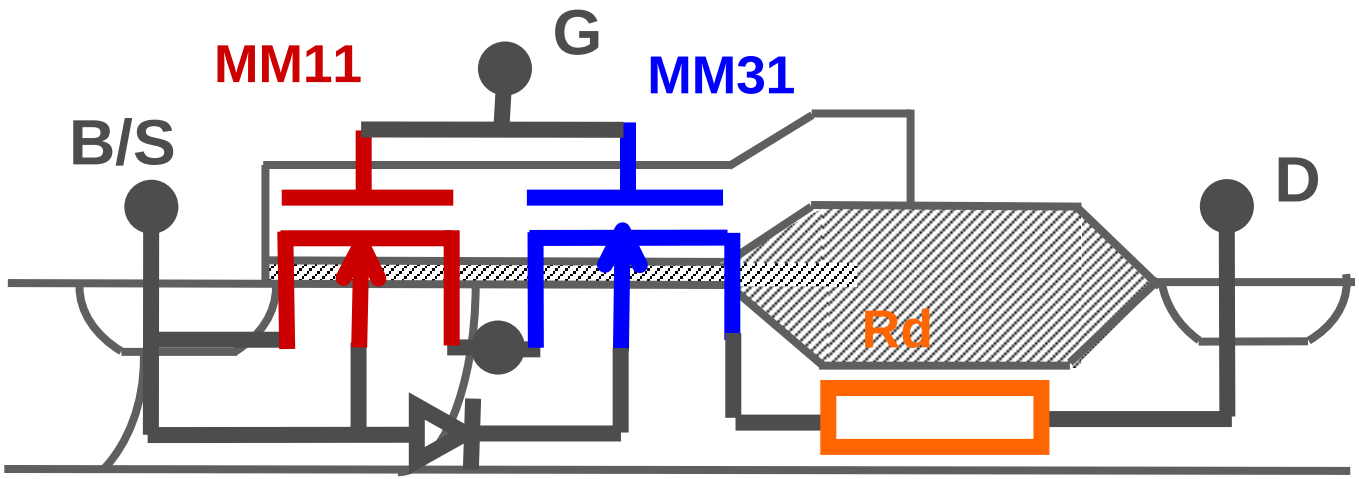

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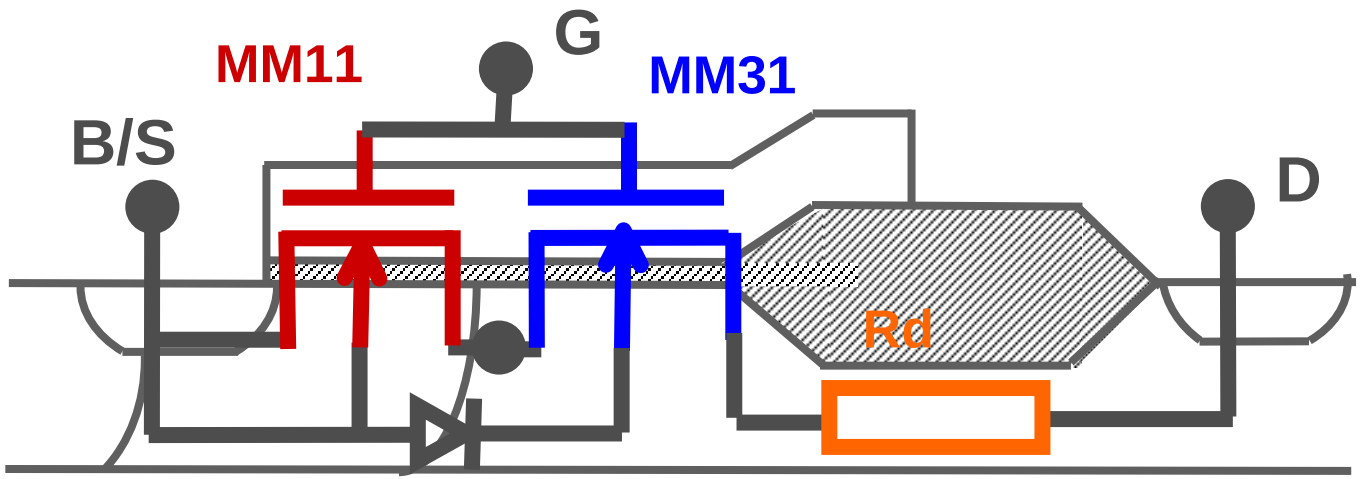

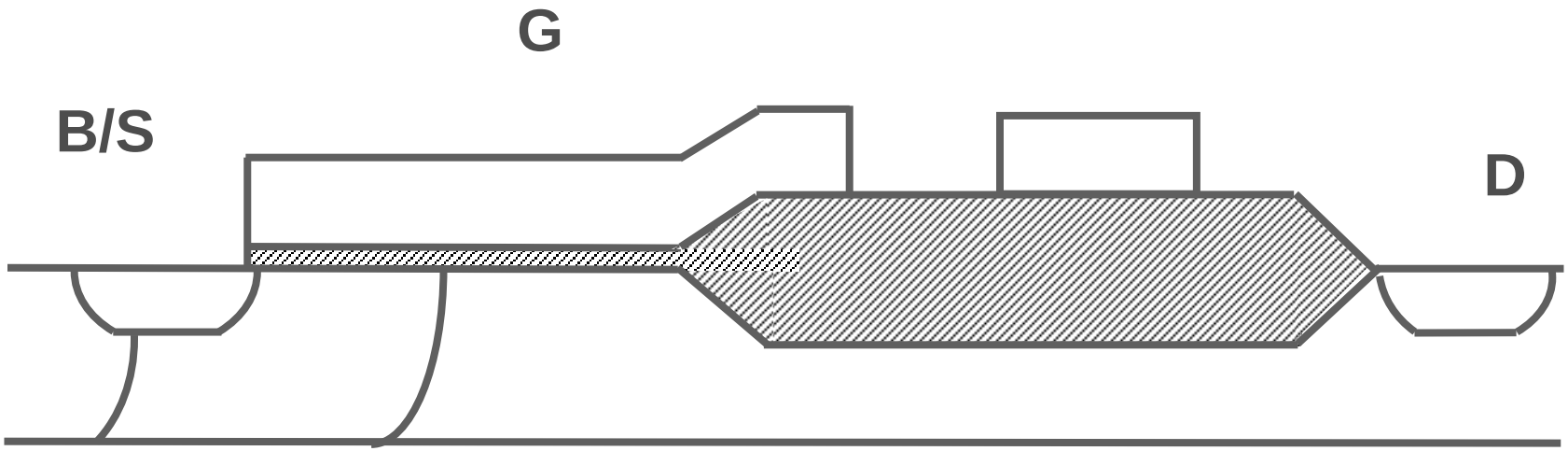

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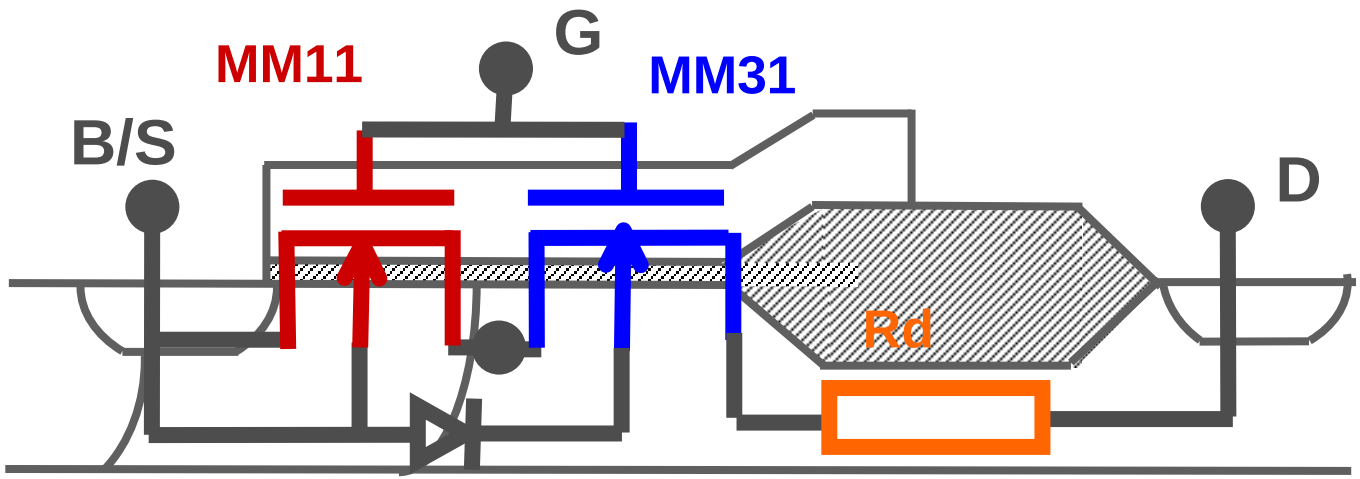

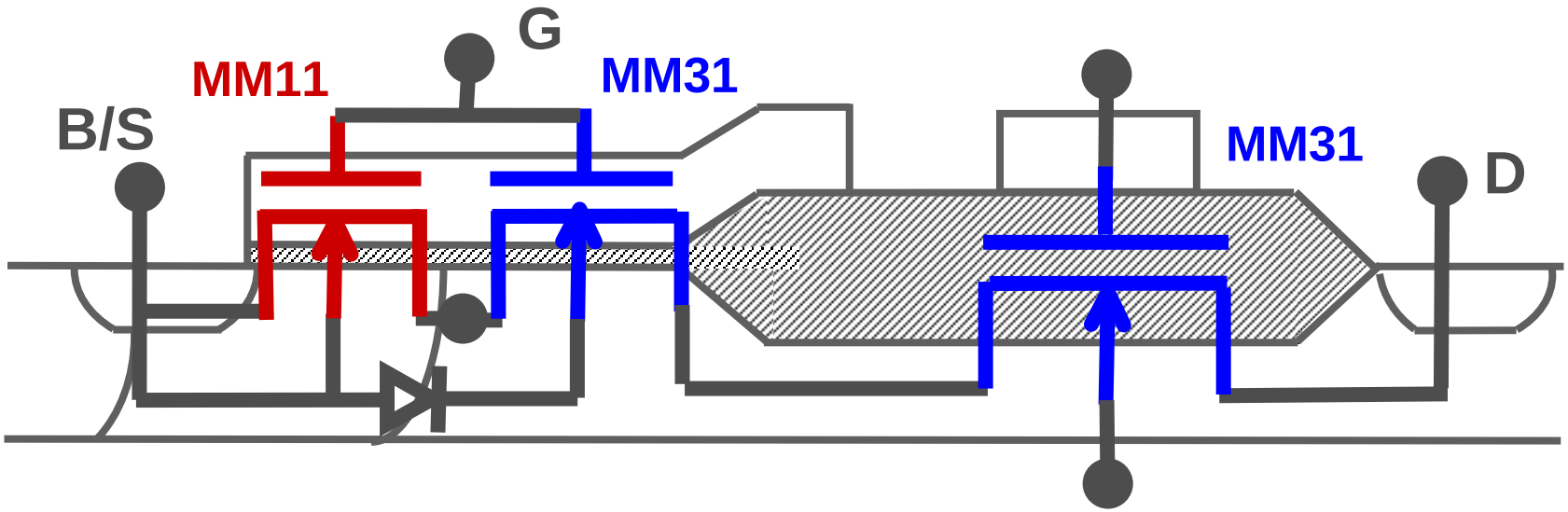

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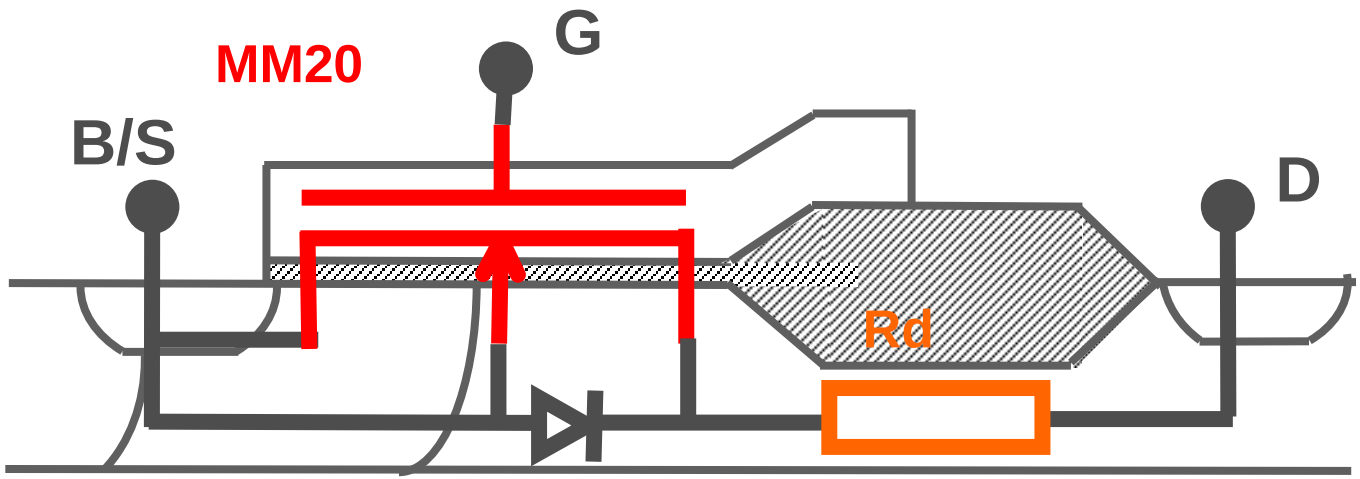
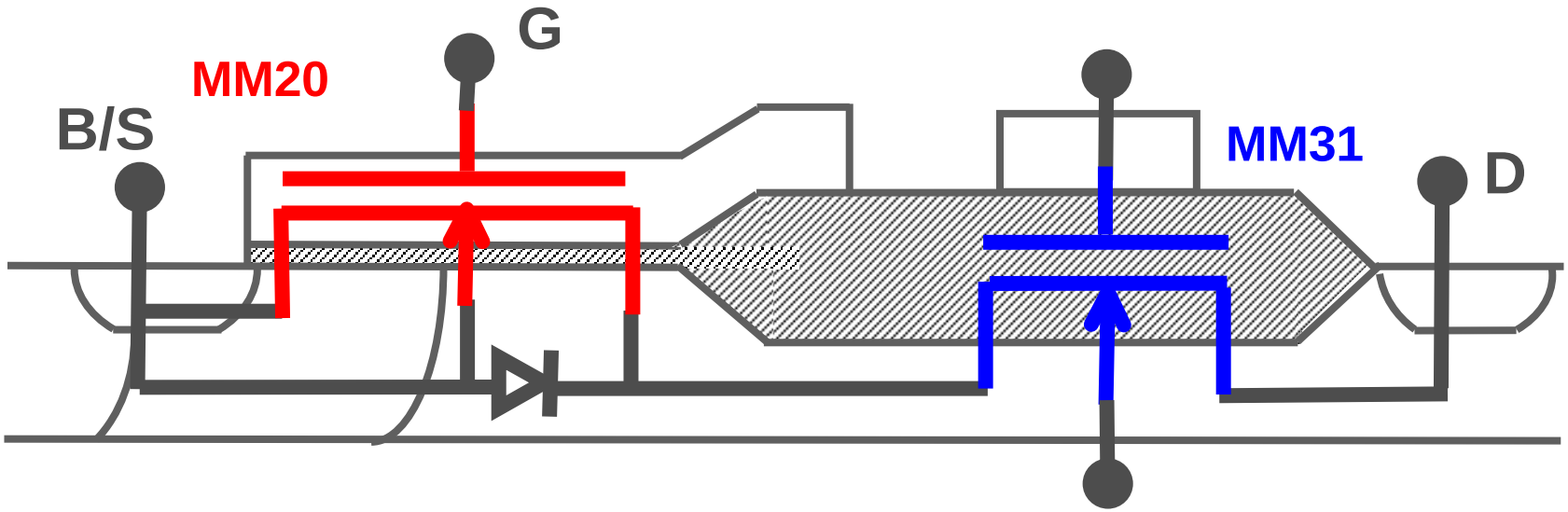
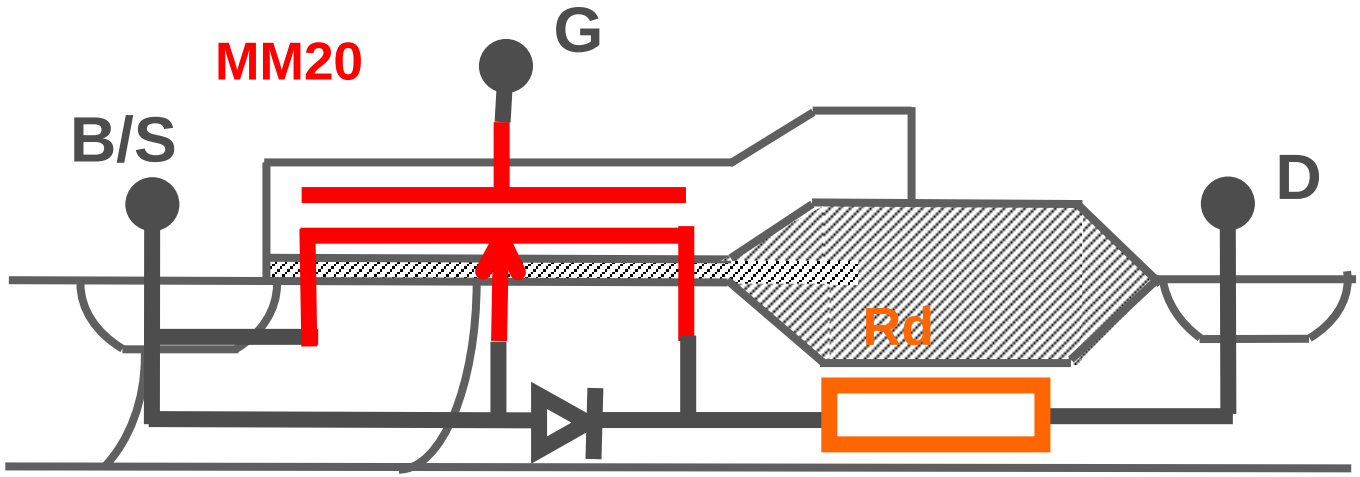




Introduction: LDMOS models



MOS Model 20:

- describes channel region + drift region under thin gate oxide
- basis building block for broad range of LDMOS

MOS Model 31: describes junction isolated drift region

MOS Model 40: describes drift region on SOI

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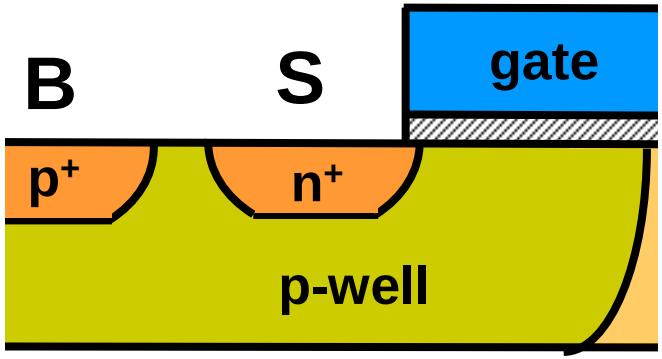
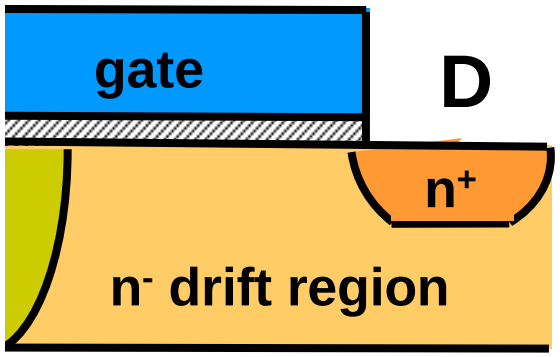
MOS Model 20: physics and features

- surface-potential based
- DC-, AC and nodal charge model
- 1/f, thermal, gate-induced noise model
- avalanche model
- geometry (length & width) scaling
- temperature scaling
- self-heating

- excellent convergence behaviour
- simulation times equal to sub-circuit models

MOS Model 20: physics and features





channel region:

- mobility reduction due to vertical electric field
- velocity saturation
- channel length modulation
- DIBL & static feedback
- avalanche

drift region:

- accumulation
- depletion
- bulk current
- mobility reduction due to vertical electric field
- velocity saturation
- avalanche

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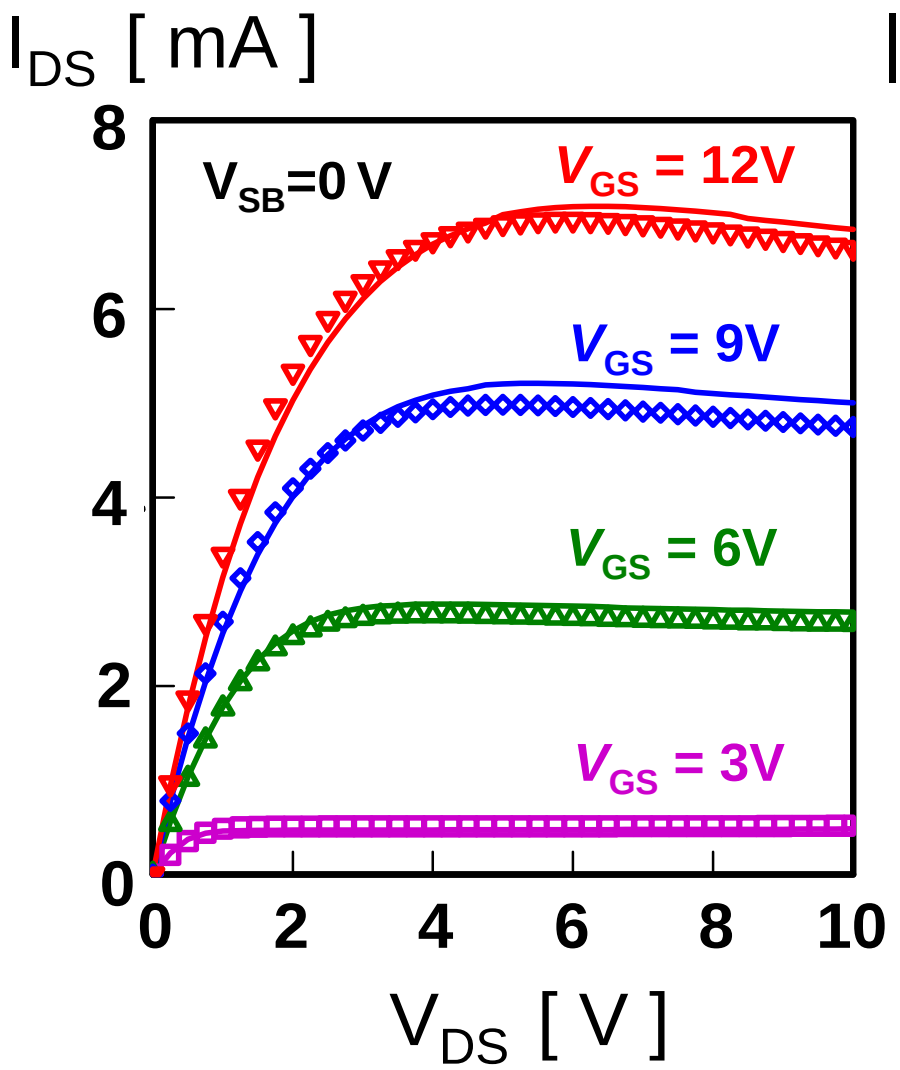
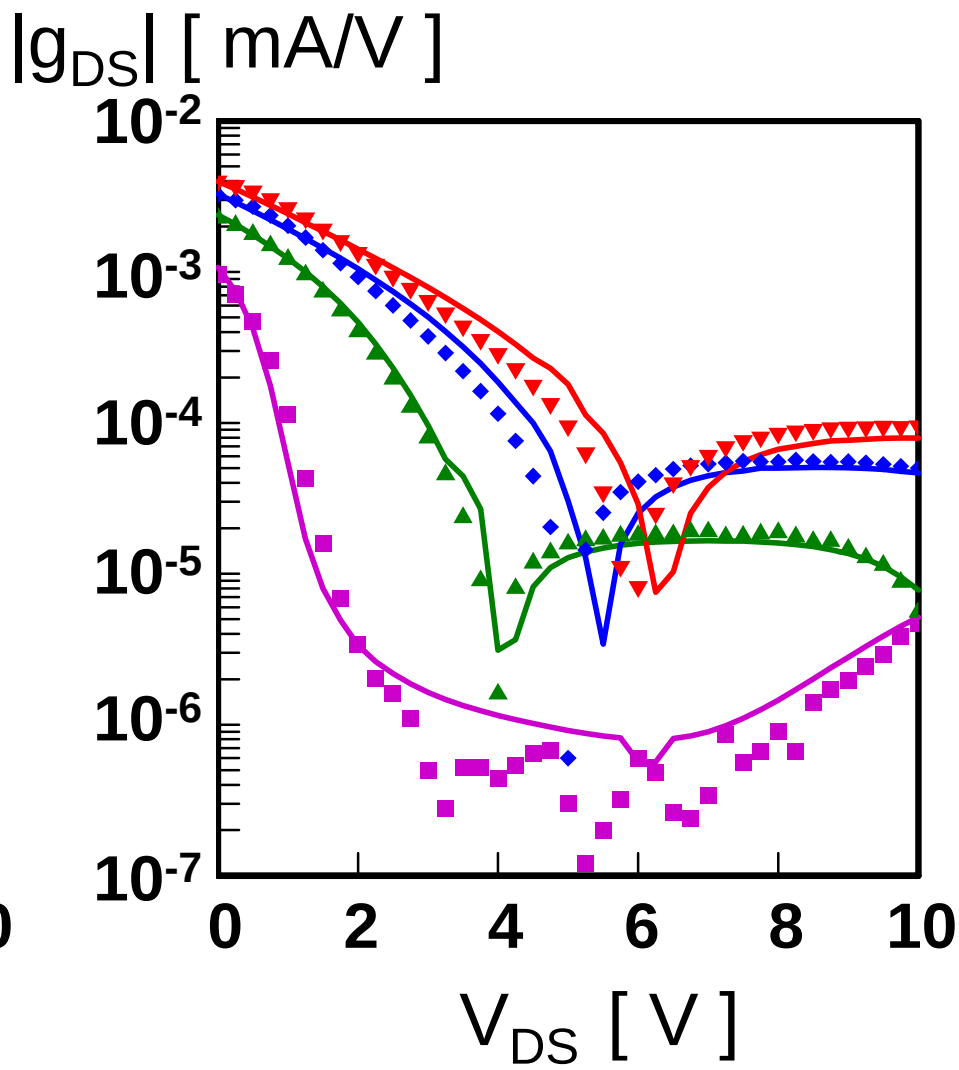
MOS Model 20: some results

12V SOI-LDMOS: T_{ox}= 38 nm, W = 17 μm, L = 1.6 μm, T = 25 °C

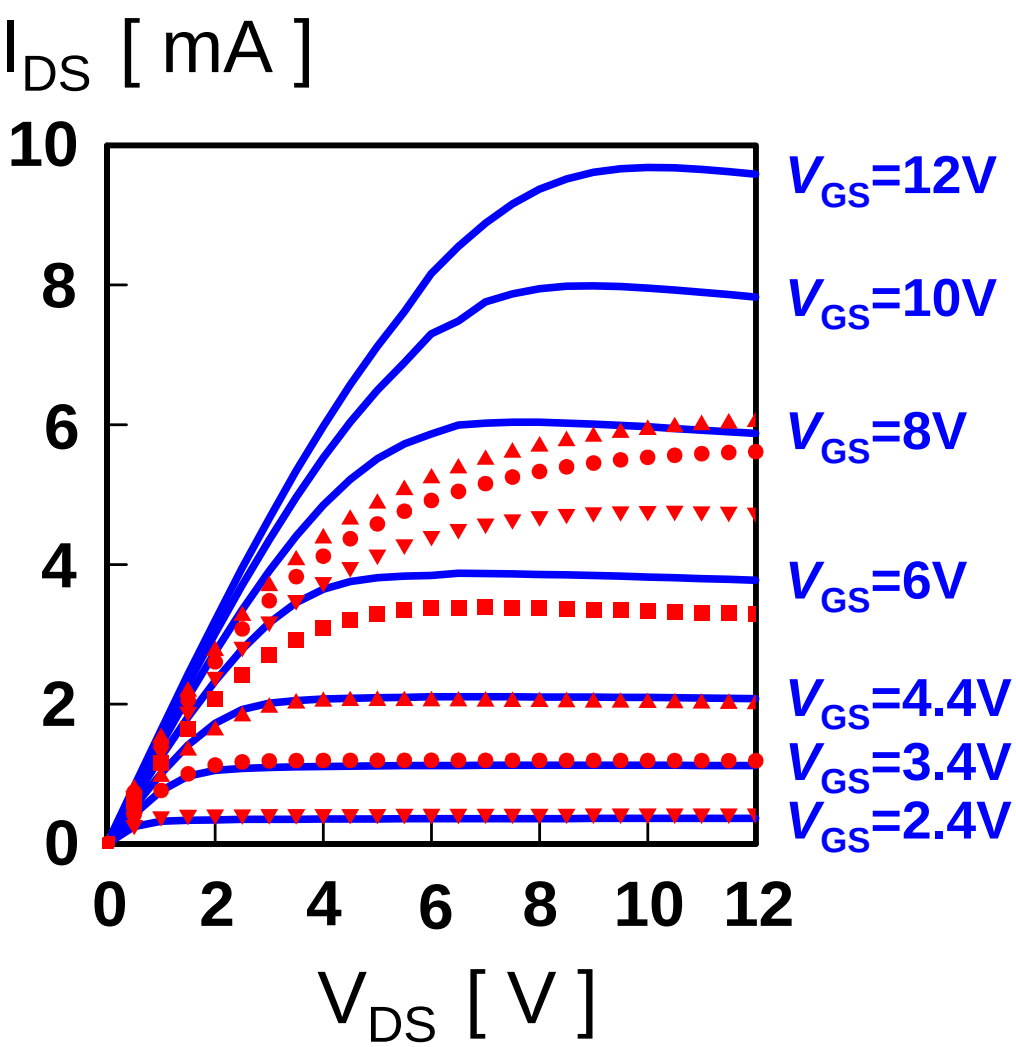




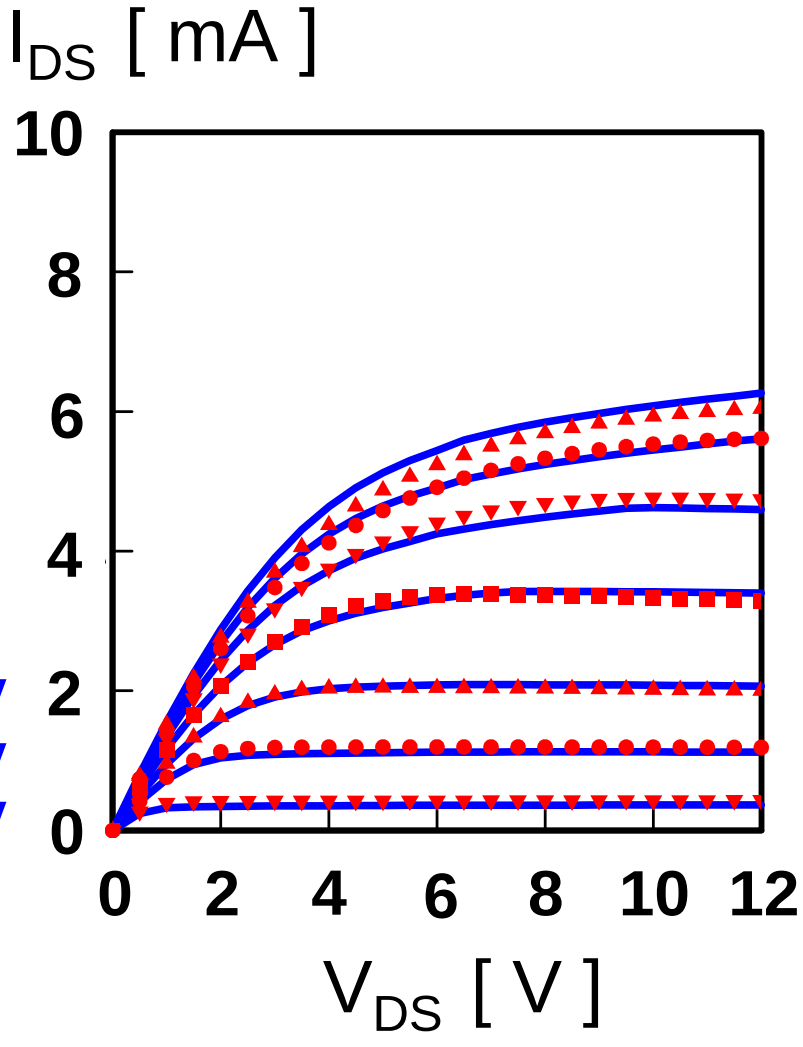
MOS Model 20: some results

60V SOI-LDMOS: T_{ox}= 38nm, W = 20µm, L = 2.6µm, L_{locos}= 3.5µm, T= 25 °C

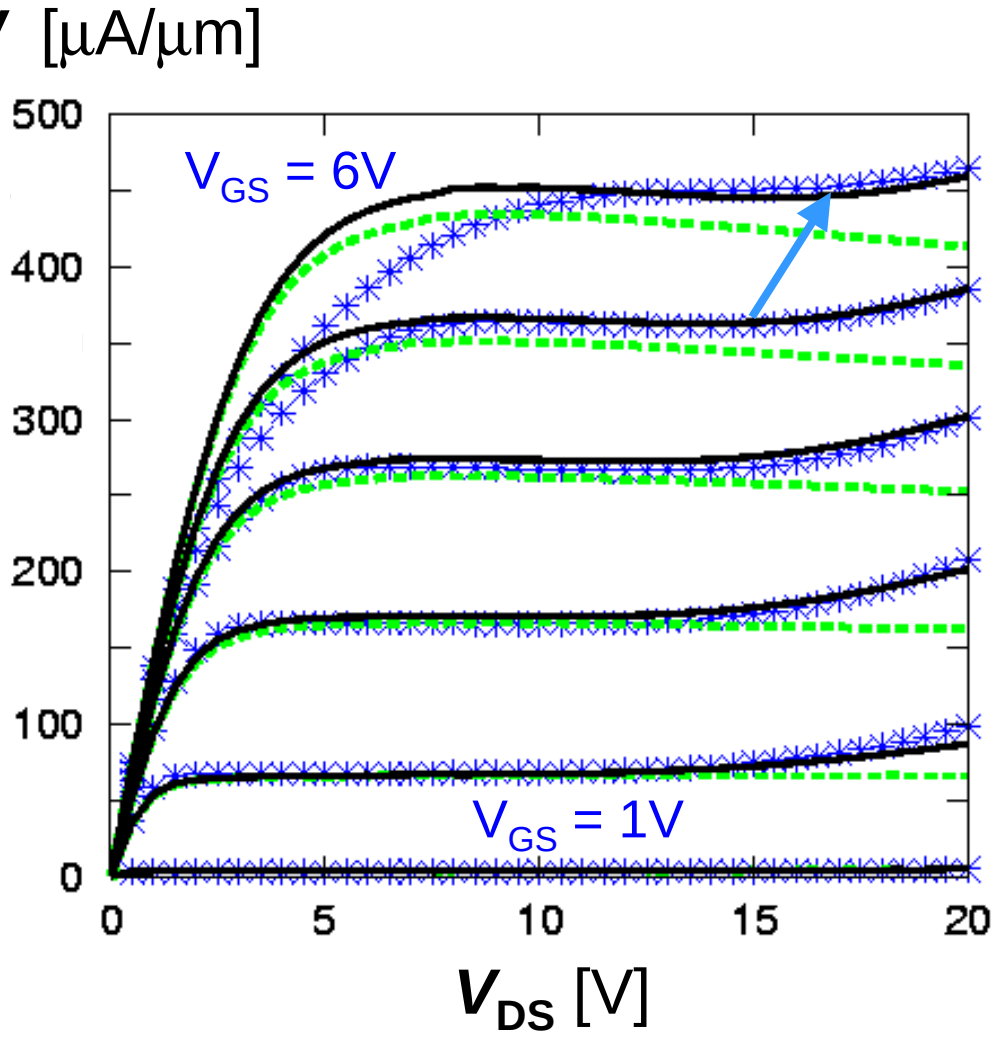
without quasi-saturation



including quasi-saturation



MOS Model 20: some results



measured

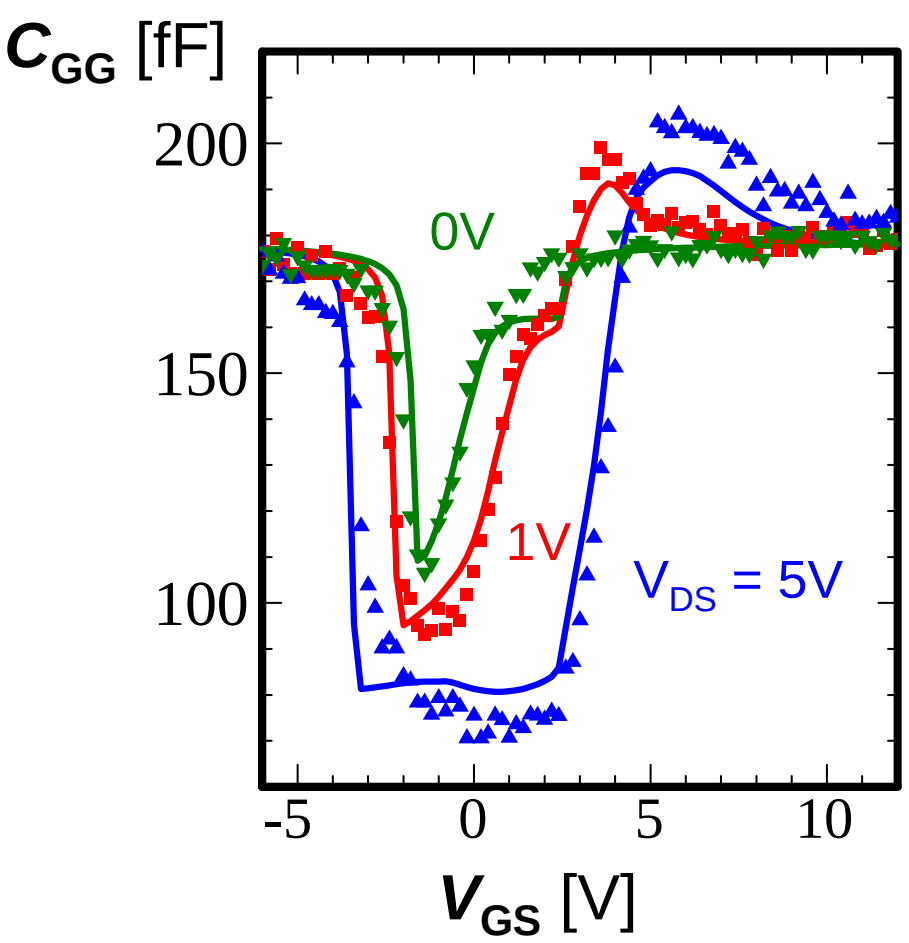
old model

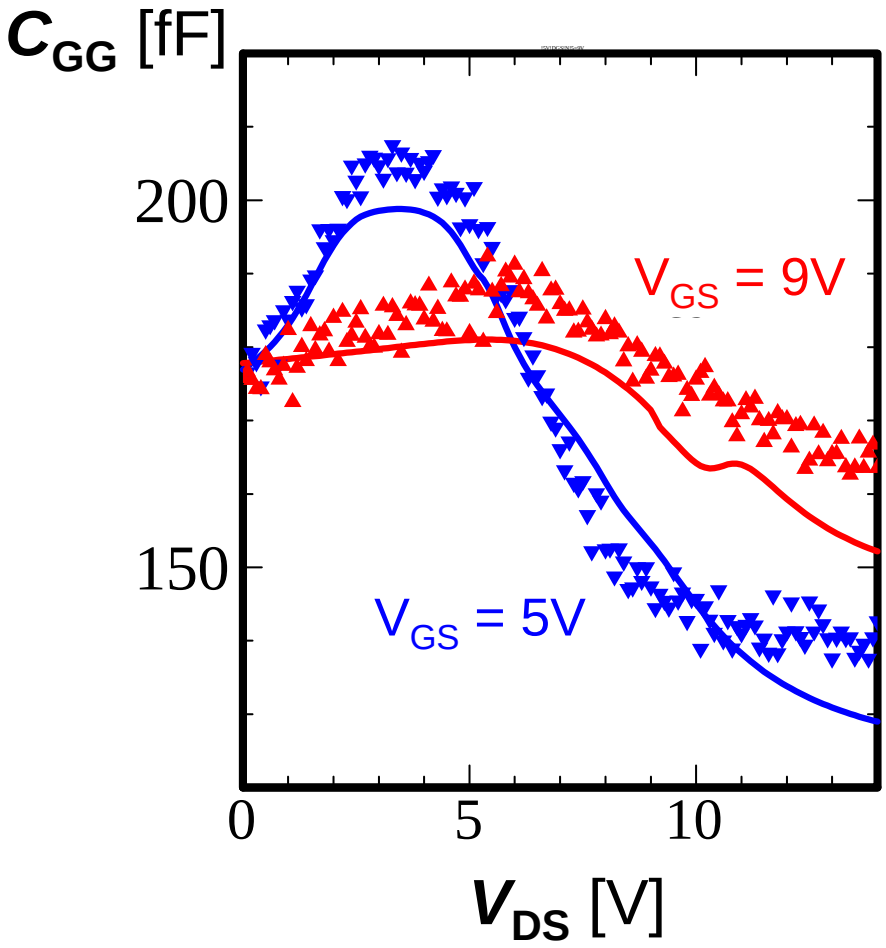
new model

avalanche current modelling is improved

MOS Model 20: some results

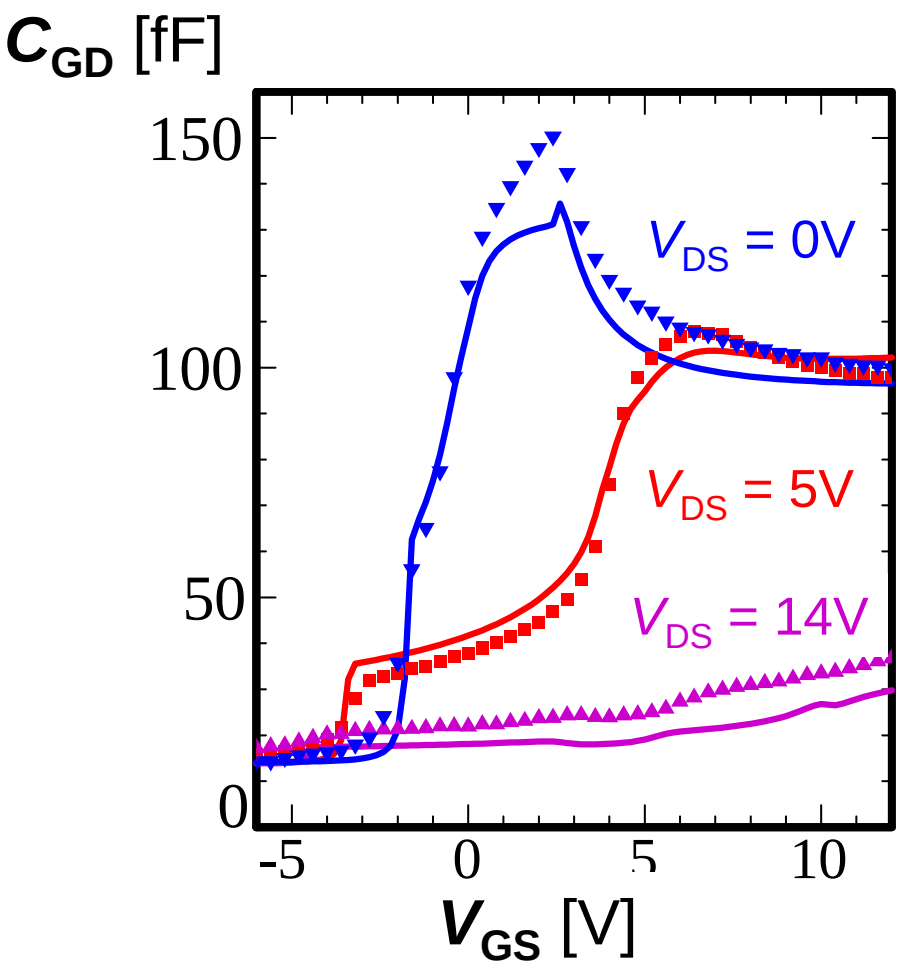
14V SOI-LDMOS: T_{ox} = 60 nm, W = 50 μm, L = 5 μm, T = 25 °C

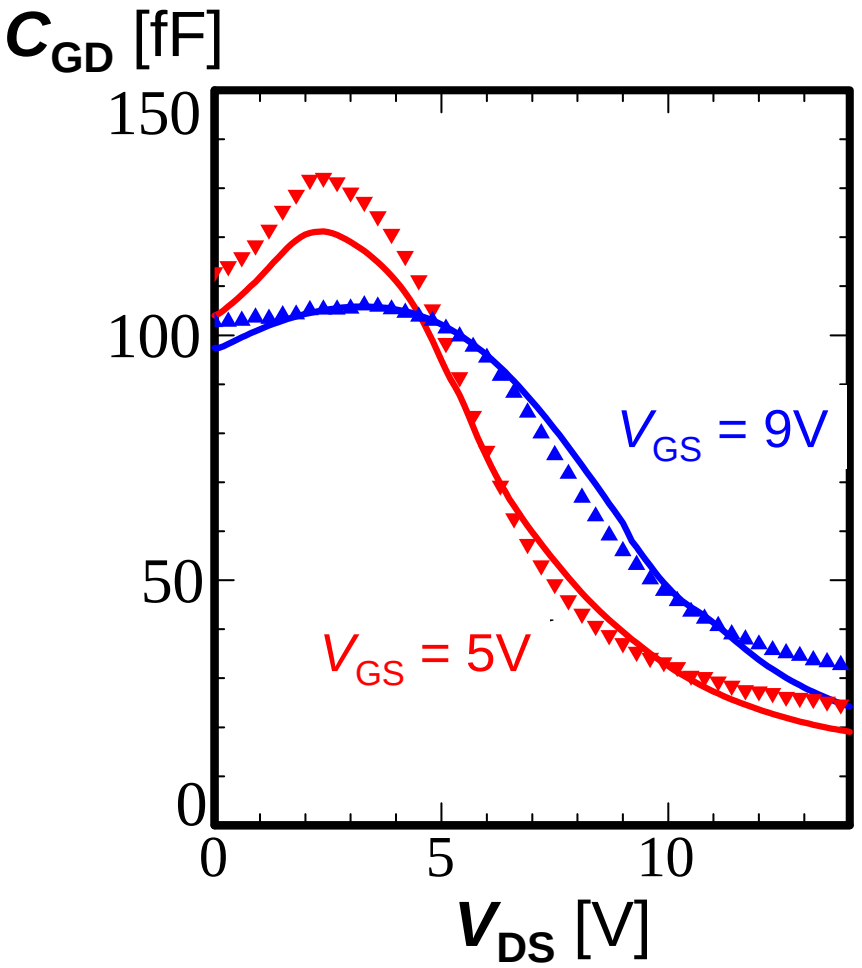




MOS Model 20: some results

14V SOI-LDMOS: T_{ox} = 60 nm, W = 50 μm, L = 5 μm, T = 25 °C





MOS Model 20: more results

- **CMC 2006 minutes and presentations:**

  www.eigroup.org/cmc/minutes/2q06_presentations/cmc_mm20_www.pdf

  www.eigroup.org/CMC/minutes/3q06_presentations/overview.pps

  www.eigroup.org/CMC/minutes/3q06_presentations/mm2002_update.pdf

- **IEEE Trans. Electron Devices:**

  - A. Aarts, N. D'Halleweyn, R. v. Langevelde,
    "A surface-potential-based high-voltage compact LDMOS transistor model", Vol. 52, No. 5, 2005
  - A.C.T. Aarts and W.J. Kloosterman
    "Compact modeling of high-voltage LDMOS Devices including quasi-saturation", Vol. 53, No. 4, 2006

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source code

C-code:

- **SimKit 2.3, level version 2002.0:**

  old avalanche model, no self-heating

  available: http://www.nxp.com/Philips_Models/high_voltage/model20

- **SimKit 2.4, level version 2002.1:**

  improved avalanche model, no self-heating

  available: http://www.nxp.com/Philips_Models/high_voltage/model20

  (since MOS Model 20, level 2002, is a test version,

  no attention is paid to backwards compatibility)

- **SimKit 2.5, level version 2002.X:**

  improved avalanche model & self-heating:

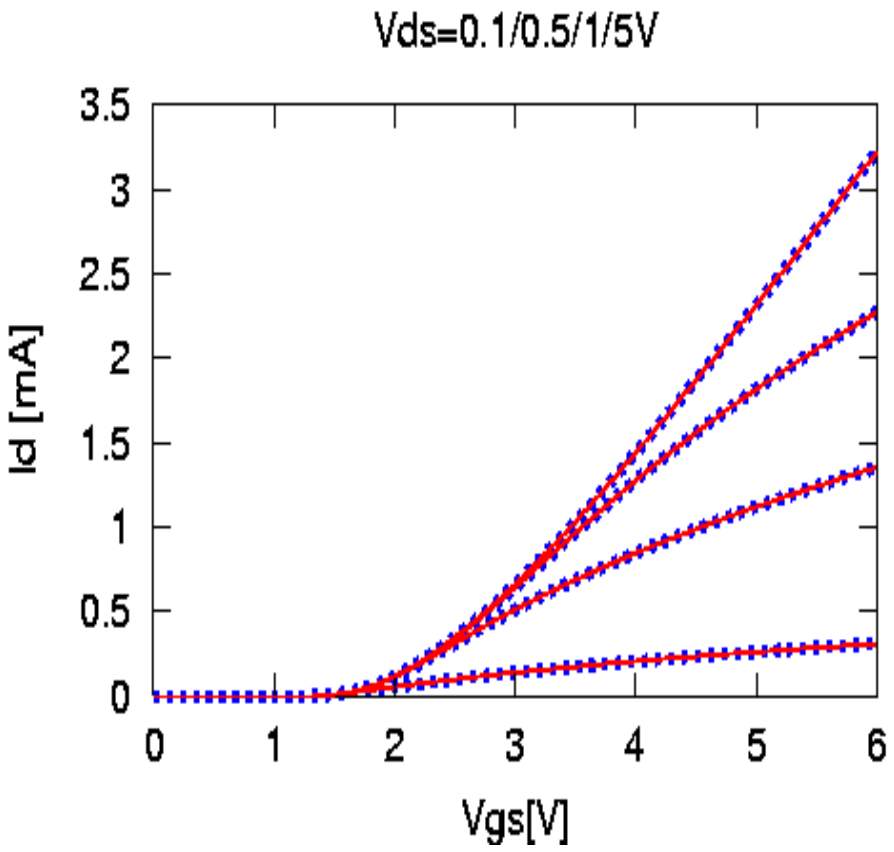
  to be released at the end of March 2007

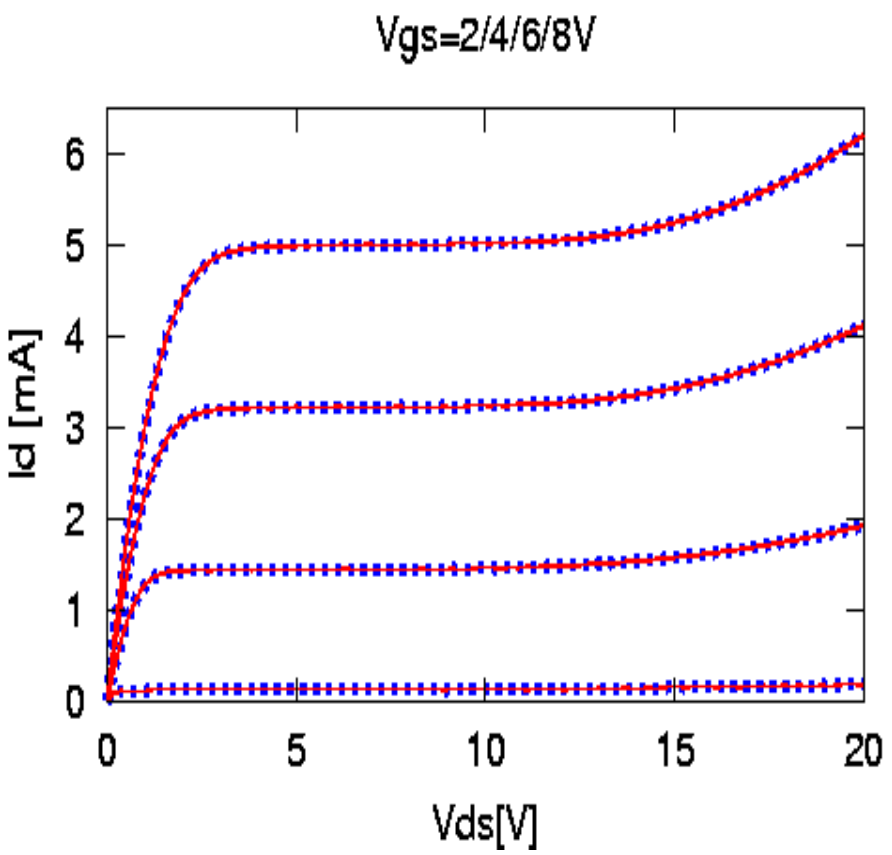
source code

Verilog-A code:

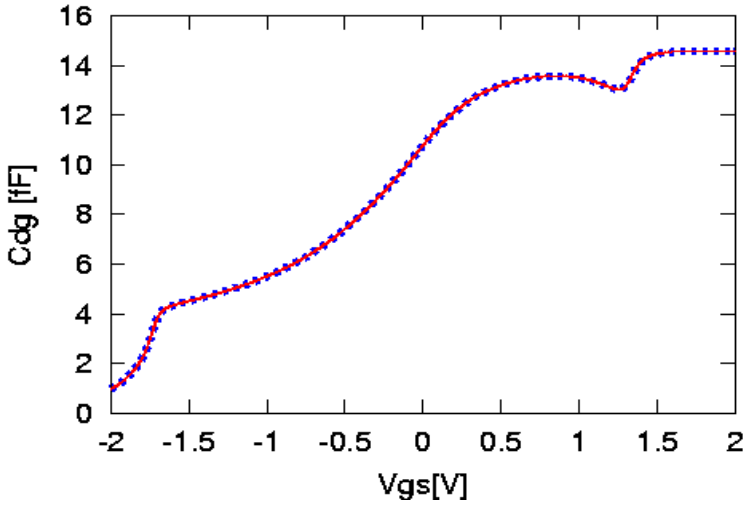
- original VA-code made by Geoffrey Coram (Analog Devices) based on documentation of level 2002.0, including self-heating
- alignment of VA-code with C-code by Alireza Tajic (NXP Semiconductors), ongoing
  - ✓ improved avalanche model has been added
  - ✓ parameter clipping has been added
  - ✓ DC analyses: in agreement with C-code
  - AC analyses: in agreement with C-code except at Vds=0
  - transient analyses: not tested yet
  - noise analyses: not tested yet
- VA-code will be released to CMC membership

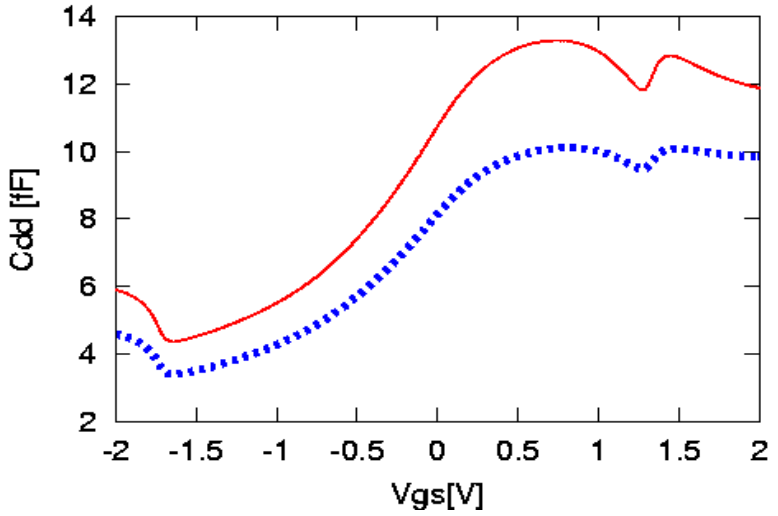
comparing C-code & VA-code: DC characteristics

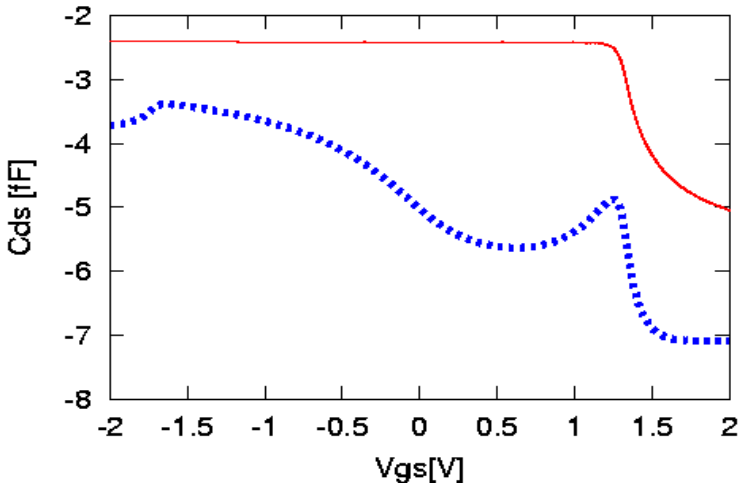


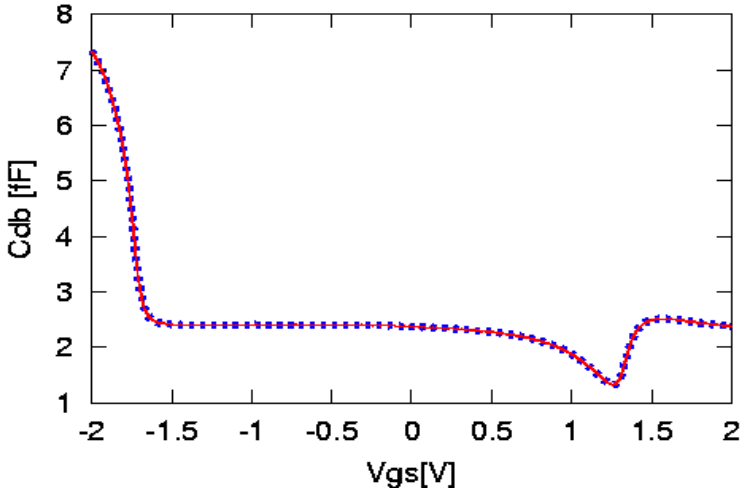


comparing C-code & VA-code: AC characteristics at Vds=0

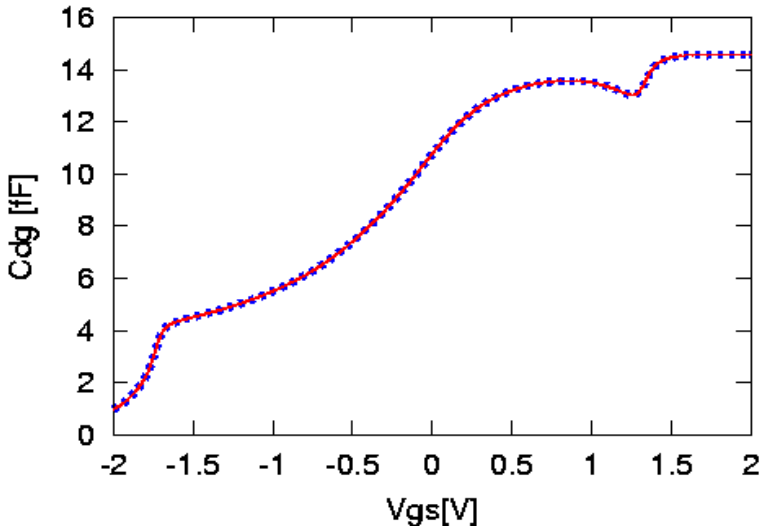


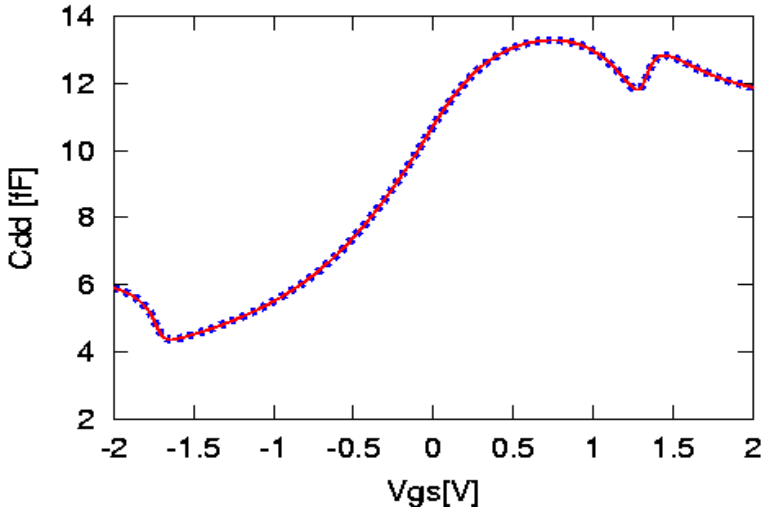


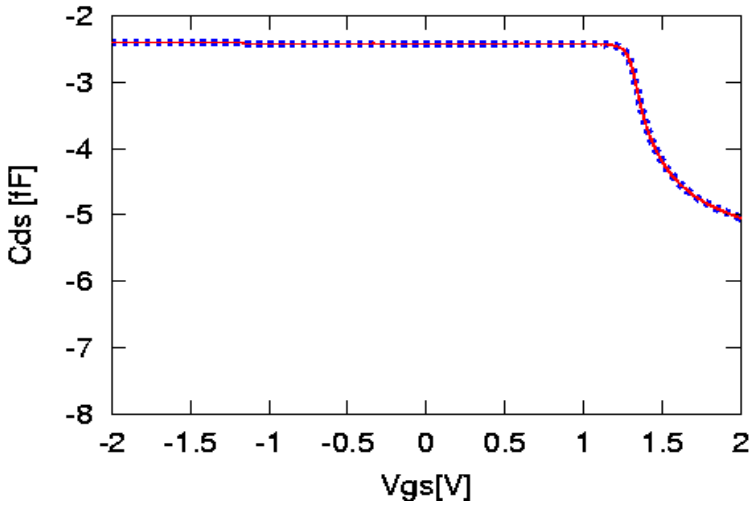


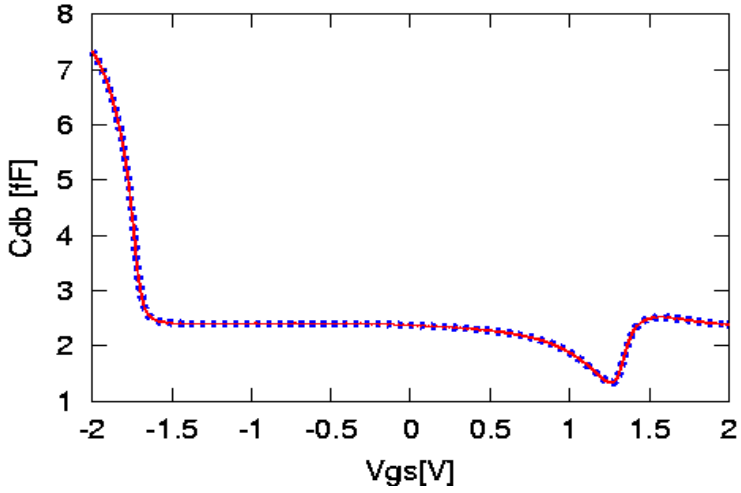


comparing C-code & VA-code: AC characteristics at Vds=1 mV









model documentation

- some errors in documentation have been found (see CMC meeting Oct. 06)
- recently updated model documentation, including the improved avalanche model, available at:

  http://www.nxp.com/acrobat_download/other/philipsmodels/m2002.pdf

Note: the link http://www.nxp.com/acrobat_download/other/philipsmodels/prtn2005_00406.pdf has NOT yet been updated

- corrections to the model documentation, to be updated in March 2007:
  - in Eq.(8.90) Φ_{BT} must be replaced by Φ_{BDT}
  - Eq.(8.213) should read

$$V_{GDi_{lim}} = V_{GDi_{t,eff}} - \mathrm{hyp}[V_{GDi_{t,eff}} - V_{T_t}; \varepsilon_7]$$

Summary

- **MM20 usable for wide variety of HV-MOS**
  - LV-LDMOS: only MM20
  - HV-LDMOS: subcircuit: MM20 serves as core
- **MM20 gives accurate results for all regimes of operation**
- **MM20 tested in many different circuits**
  - excellent convergence behaviour
- **MM20 source code & documentation available**

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