

Simplified Control for Parasitic Gate, Source and Drain Resistance

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**Mentor
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The Problem

- **Foundries are asking parasitic extractors to determine gate, source and drain resistances from the layout**
- **Control of R_g , R_s and R_d in the transistor model is scattered among several different parameters**
 - **NRS, NRD**
 - **RGEOMOD**
 - **RGATEMOD**
- **Risk of double counting parasitic R's**

Goal

- **Provide a single instance variable to control all parasitic terminal resistance (R_g , R_s , R_d)**
- **Allow extraction users the control over interaction of extractor and models they've requested**
- **Device and parasitic extraction better coordinated**
 - **Parasitic extractors determine when to extract R_g , etc. based on single device extraction parameter**
 - **Reduce the possibility of double counting**

Reasoning

- **SPICE models not under control of design engineers**
- **LVS / Extraction commands and options *are* under their control (sometimes)**
- **Currently limited flexibility**
 - **Not setting NRS/NRD just means that RGEOMOD has control. Must edit model card to turn this on/off**
 - **Rg controlled by model card parameter only (RGATEMOD), no local control**

Proposal

- **Single instance parameter that controls when model computes Rg, Rs, and Rd**
- **RTERM 0 | 1 | 2**

RTERM	Rgate handled by model	Rsource / Rdrain handled by model
0 (default)	Yes	Yes
1	No	Yes
2	Yes	No
3	No	No

Compatibility with Existing Parameters

- **NRS / NRD still have precedence over RGEOMOD if RTERM not set**
- **RTERM has precedence over NRS / NRD and RGEOMOD**
- **RTERM has precedence over RGATEMOD**

Summary

- **Single point of control for parasitic terminal resistance**
- **Increased flexibility for design engineers**
- **Supports foundry requirements**
- **Reduces or eliminates possibility of double counting**
- **Simplifies / automates interaction between parasitic and LVS device extraction**