

RGCON is 1 for a gate contacted at one end and 2 for a gate contacted at both ends.

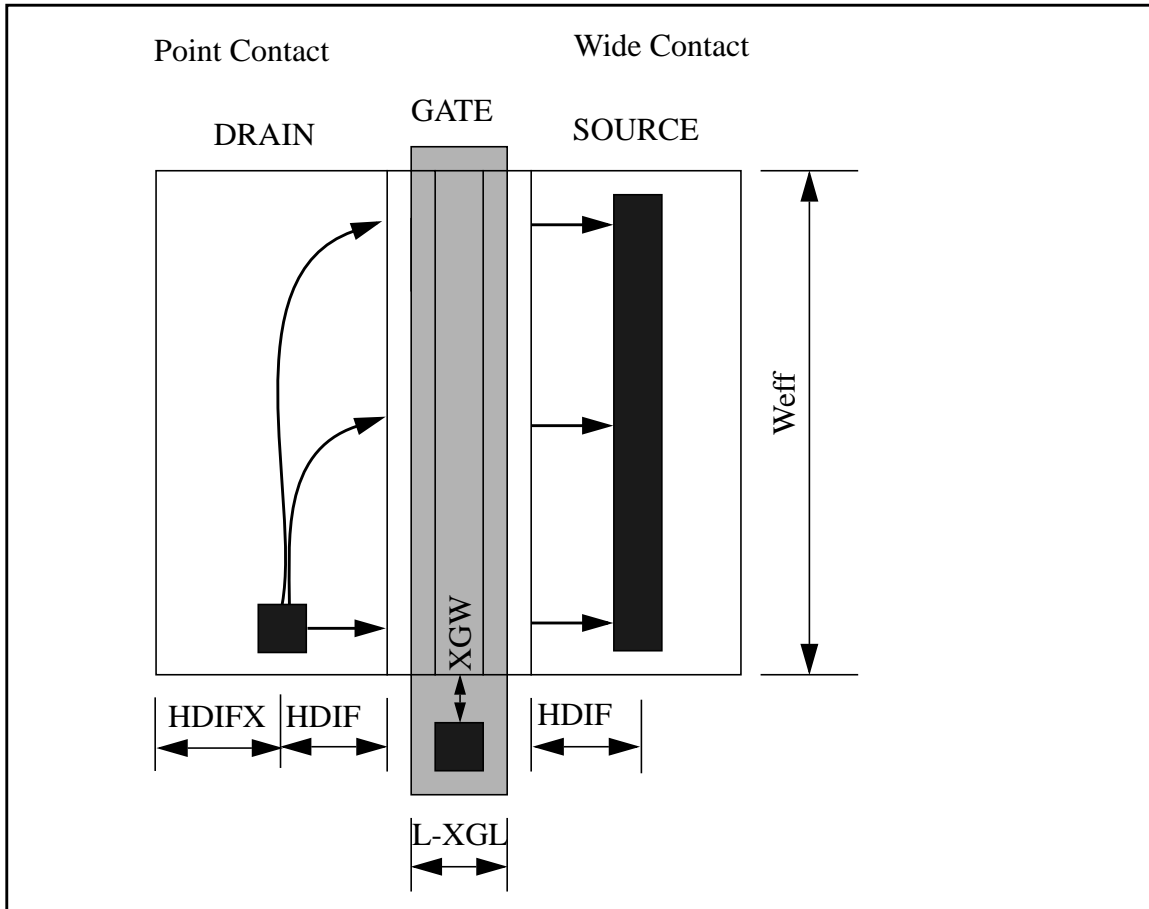


FIGURE 2. Geometry for resistance calculations

$$R_{source} = NRS * RSH$$

$$R_{drain} = NRD * RSH$$

For contacts for which NRS/NRD are not specified the following procedure applies.

The parameter RGEO selects no resistor or one of two calculation methods for the each of the source and the drain junctions as follows:

**TABLE 4.**

<b>RGEO Value</b>	<b>Source Calculation</b>	<b>Drain Calculation</b>
0	No Resistor	No Resistor
1	Wide Contact	Wide Contact
2	Wide Contact	Point Contact
3	Point Contact	Wide Contact
4	Point Contact	Wide Contact

Wide Contact

$$R_{source} = RSH * HDIF / W_{effc}j$$

$$R_{drain} = RSH * HDIF / W_{effc}j$$

Point Contact

$$R_{source} = RSH * W_{effc}j / (3 * (HDIF + HDIFX))$$

$$R_{drain} = RSH * W_{effc}j / (3 * (HDIF + HDIFX))$$

## Gate RESISTANCE

Add new parameter RGMOD for selecting whether or not gate series resistance is calculated.

Add new parameters XGW, XGL, RSHG and RGCON to calculate the gate series resistance.

If RGMOD=0 no gate series resistor is generated. If RGMOD=1 then the gate resistance is calcu-

**TABLE 5. New Parameters for Gate Resistance Calculation**

<b>Parameter</b>	<b>Specified on</b>	<b>Default</b>
RGMOD	device call	0
XGW	.model card	0
XGL	.model card	0
RSHG	.model card	0
RGCON	.model card	1

lated as follows:

$$R_{gate} = RSHG * (XGW + W_{effc}j / (3 * RGCON)) / (RGCON * (L - XGL))$$

The following figure illustrated the isolated, shared and merged geometries for junction area and perimeter calculations.

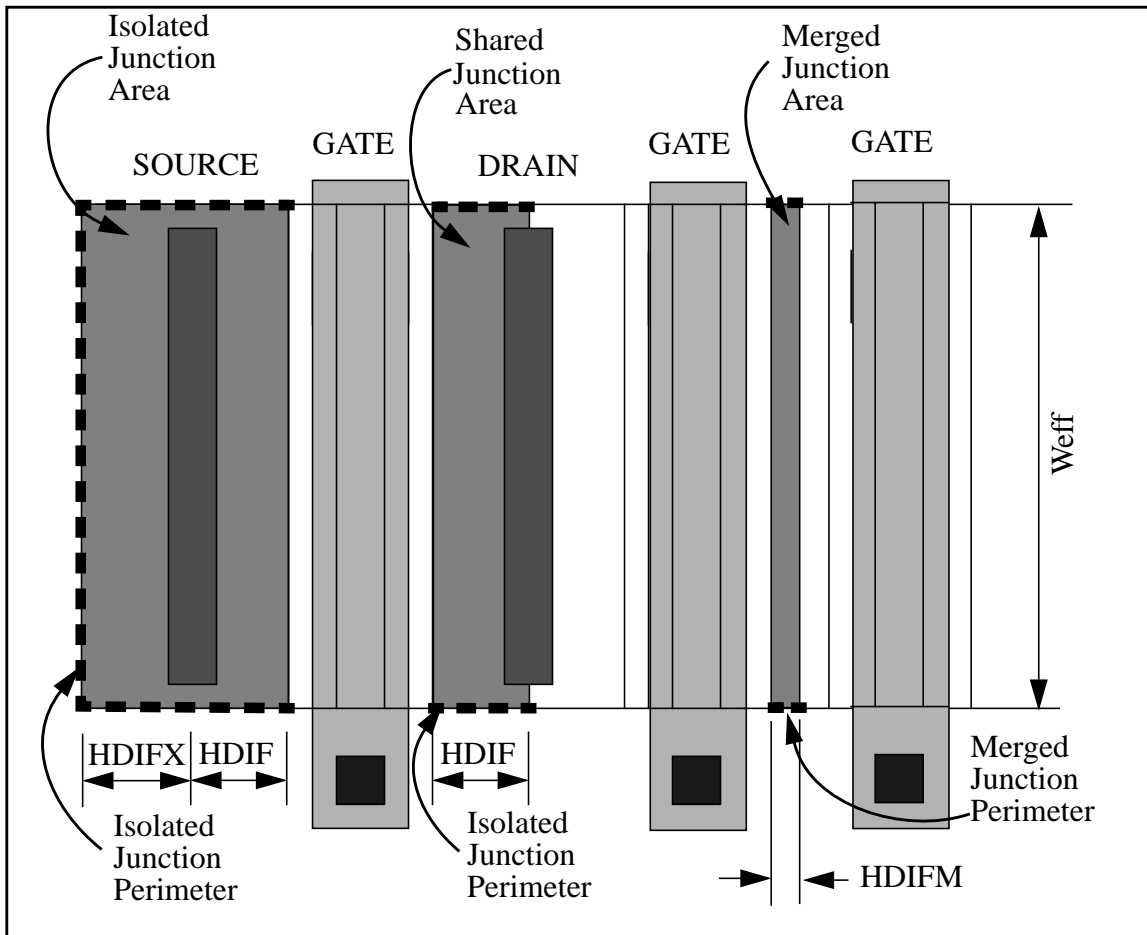


FIGURE 1. Junction Area and Perimeter Calculations

## Source/Drain RESISTANCE

Add new parameter RGEO for selecting how series resistance is calculated.

TABLE 3. New Parameters for Series Resistance Calculation

Parameter	Specified on	Default
RGEO	device call	0

### Calculation of Series Source/Drain Resistance

If none of RGEO, NRD and NRS are specified then RGEO defaults to 0 and no resistors are generated.

If either of NRD and NRS is specified, regardless of whether or not RGEO is specified, then the corresponding series resistance is calculated as follows:

$$\underline{\underline{\text{PERMOD} = 1}}$$

$$\text{ASeff} = \text{AS}$$

$$\text{PSeff} = \text{PS} - \text{Weffc}j$$

$$\text{ADeff} = \text{AD}$$

$$\text{PDeff} = \text{PD} - \text{Weffc}j$$

If any of AS, PS, AD or PD are not specified the corresponding value is calculated using the equation selected by the parameter GEO. This table shows the source and drain calculation methods associated with various values of GEO.:

**TABLE 2. Area Calculations Based on GEO Values**

<b>GEO Value</b>	<b>Source Calculation</b>	<b>Drain Calculation</b>
0	Isolated	Isolated
1	Isolated	Shared
2	Shared	Isolated
3	Shared	Shared
4	Isolated	Merged
5	Shared	Merged
6	Merged	Isolated
7	Merged	Shared
8	Merged	Merged

Isolated junction area calculation

$$\text{ASeff} = (\text{HDIFX} + \text{HDIF}) * \text{Weffc}j$$

$$\text{PSeff} = 2 * (\text{HDIFX} + \text{HDIF}) + \text{Weffc}j$$

$$\text{ADeff} = (\text{HDIFX} + \text{HDIF}) * \text{Weffc}j$$

$$\text{PDeff} = 2 * (\text{HDIFX} + \text{HDIF}) + \text{Weffc}j$$

Shared junction area calculation

$$\text{ASeff} = \text{HDIF} * \text{Weffc}j$$

$$\text{PSeff} = 2 * \text{HDIF}$$

$$\text{ADeff} = \text{HDIF} * \text{Weffc}j$$

$$\text{PDeff} = 2 * \text{HDIF}$$

Merged junction area calculation

$$\text{ASeff} = \text{HDIFM} * \text{Weffc}j$$

$$\text{PSeff} = 2 * \text{HDIFM}$$

$$\text{ADeff} = \text{HDIFM} * \text{Weffc}j$$

$$\text{PDeff} = 2 * \text{HDIFM}$$

## Capacitance:

Add parameters PERMOD (Perimeter Model) and GEO to select how junction capacitance is calculated. Add parameters HDIF, HDIFX, HDIFM, XW, for calculating junction capacitance.

**TABLE 1. New Parameters for Junction Capacitance Calculation**

Parameter	Specified on	Default
HDIF	.model card	0
HDIFX	.model card	HDIF
HDIFM	.model card	0
DWJ	.model card	0
PERMOD	.model card	1
GEO	.model card	0
GEO	device call	GEO on.model card

Calculation of junction capacitance:

$$C_{source} = C_j(T,V) * A_{seff} + C_{jsw}(T,V) * P_{seff} + C_{jswg}(T,V) * W_{effcj}$$

$$C_{drain} = C_j(T,V) * A_{deff} + C_{jsw}(T,V) * P_{deff} + C_{jswg}(T,V) * W_{effcj}$$

where  $C_j(T,V)$ ,  $C_{jsw}(T,V)$  and  $C_{jswg}(T,V)$  are the junction capacitance coefficients including the effects of temperature and junction voltage.

Similarly junction diode currents are calculated from the effective areas and perimeters as follows:

$$I_{sbs} = J_s * A_{seff} + J_{sw} * (P_{seff} + W_{effcj})$$

$$I_{sbd} = J_s * A_{deff} + J_{sw} * (P_{deff} + W_{effcj})$$

$$W_{effcj} = W_{design} - 2 * dw_j$$

$A_{seff}$ ,  $P_{seff}$ ,  $A_{deff}$  and  $P_{deff}$  are calculated according the equations below depending on the choice of PERMOD.

If AS, PS, AD or PD are given on the model call then the corresponding effective value depends on the value of PERMOD. The calculations are follows:

$$\underline{PERMOD = 0}$$

$$A_{seff} = AS$$

$$P_{seff} = PS$$

$$A_{deff} = AD$$

$$P_{deff} = PD$$

## Proposal for BSIM3 definitions of Parasitics

The purpose of this proposal is to standardized the specification of process information that effects parasitic capacitances and resistances associated with the FET. By specifying the equations used to calculate the capacitance and resistance the associated parameters are unambiguously defined. Any designer using a BSIM3 model will get the estimate of the parasitic that the model builder intended regardless of the simulator he/she is using.

I drew the following conclusions from the discussions at the compact model council meeting on May 15, 1998:

1. We do want to include definitions of parasitic C and R calculations for simulations before physical design including circuit optimization. For extracted net lists these calculations are not necessary
2. We want it to be as simple as possible.
3. We want to choose the best formulation regardless of whether that makes BSIM3 compatible or incompatible with HSPICE.
4. We do need to support two definitions of the parameters PS and PD, one including the gate edge perimeter and one excluding the gate edge
5. Series resistance of any Ldd/extensions is best handled within the Ids calculations possibly using the model enhancements suggested by Siemens.

I revised this proposal based on these ideas. Specifically:

1. To calculate Weff for parasitic calculations I have introduced a new parameter dwj similar to dwc.

$$W_{effc_j} = W_{design} - 2 * dw_j$$

$$+ w_{lc} / (L^{w_{lnc}}) + w_{wc} / (W^{w_{wnc}}) + w_{wlc} / ((L^{w_{lnc}}) * (W^{w_{wnc}}))$$

This is not compatible with HSPICE but is consistent with other BSIM3 width calculations. Based on the feed back I received I have included the *capacitance* geometric adjustment factors (w<sub>wc</sub>, w<sub>lc</sub>, etc.).

2. I have eliminated the instance specific parameters HDIFS, HDIFD, etc. in the interest of simplicity. Since these calculations are intended for simulations before physical design such device specific information would not generally be available.
3. I have eliminated the use of ACM which is an HSPICE parameter. I have added the parameter PERMOD which takes values of 0 or 1 depending on whether or not the parameters PS and PD include the perimeter length along the device gate.

By default (no parameters on the device call) this procedure produces junction capacitors but no series resistors.