

# Minutes of Compact Model Council Meeting

October 13, 2005 Face-to-Face Meeting in Santa Barbara, CA

Companies and Universities in Attendance:

Agere, Agilent, ADI, Atmel, Broadcom, Cadence, Cypress Semiconductor, TU-Delft, Evolvable Systems Research, Freescale, Fujitsu, Hiroshima University, IBM, Infineon, Intel, Intersil, STARC, Jazz Semiconductor, NEC, Panasonic, Pennsylvania State University, Philips, Renesas, RF Micro Devices, Samsung, Sharp Corporation, Silvaco, Sony, SRC, ST Microelectronics, ROHM, Synopsys, TI, Toshiba, UC-Berkeley, UC-San Diego, UMC, Xpedion Design Systems, Elpida Memory, University of Arkansas, National Semiconductor, Mentor Graphics

## 1. Membership Review (Joe Watts - IBM)

Total membership is now 32. Cypress Semiconductor and Xpedia joined since the previous meeting.

## 2. Treasurers Report (Robert Lomenick - Intersil)

There will be a 2005 budget surplus due to the recent addition of new members. Robert reviewed the officers' suggestions for how to spend the surplus. See presentation for details.

Other suggestions from the floor for how to spend the surplus were 1) develop an additional BJT model, 2) move external RF subcircuit network into core MOSFET model, and 3) fund Verilog-a compiler improvements.

Action Item:

Joe Watts will email a draft proposal to CMC members for spending 2005 budget surplus prior to the December meeting.

For 2006 dues will remain at \$15,000. Robert reviewed the officers' proposal for the 2006 budget. There were no objections. There was a suggestion to fund development of a standard corner model methodology for the next generation standard MOSFET model.

## 3. 2006 Officers

Members unanimously decided to keep the same officers for 2006-7.

## 4. Implementation of Standard Models

Agilent, Cadence, Synopsys representatives presented status of all standard models in their simulation tools. See their presentation slides for details.

Synopsys also showed a new high-voltage MOSFET model they developed. See presentation slides for details. The model is not public domain.

Silvaco reported status of standard model implementations. No slides shown.

#### 5. Mextram Update (Paul Humphries – ADI)

See Paul's slides on working convergence problems through Delft and Philips.

TU-Delft gave an update on Mextram support, including how they QC the Simkit and Verilog-a model code. See slides for details.

TI gave an overview of Mextram issues and enhancement requests. See slides for details.

#### 6. HiCUM (Dave Sheridan - IBM)

Michael Schroter presented an update on HiCUM support. See slides for details.

ADI presented results of simulator comparisons of 2.1. See slides for details.

Agilent and Synopsys presented issues found with HiCUM 2.1. See presentations for details.

Members were reminded that HiCUM level-0 is not a CMC standard.

The CMC made a decision to focus on HiCUM 2.2, not 2.1. This is a reversal of the decision made at the 2Q05 meeting. It was explained at the meeting that 2.2 is backward compatible with 2.1 and contains significant fixes and enhancements.

#### Action Item:

Michael Schroter will add a flicker noise switch and a 3-way instance switch for self-heating to HiCUM 2.2: 1) off, 2) main components only, 3) all components. The model version number will increment to 2.2c.

#### 7. Model Release Procedures

Weidong Liu (Synopsys) volunteered to chair this new subcommittee or merge it with the QA subcommittee. Ivan Pesic, Rick Poore, Dick Klaassen, and Yutao Ma volunteered for this committee.

#### Action Item:

Rob Jones and Doug Weiser (new co-chairs of the QA subcommittee) will decide with Weidong Liu if they want to simply merge model release procedure effort into the QA subcommittee.

Action Item:

The Model Release Procedure subcommittee / QA Subcommittee will generate a procedure for releasing model updates: version numbering scheme, contents of release, etc. CMC-sponsored universities will be expected to follow this procedure.

8. Verilog-a Status Report (Colin McAndrew – Freescale)

See presentation slides for details of status of Verilog-a in various simulators.

9. Code Requirements for CMC Standard Models

See CMC website for presentation slides on this topic.

An issues list was generated on this topic. See this list on the website.

Action Item:

Colin McAndrew, Ivan Pestic, Geoffrey Coram, Min-Chie Jeng, and Weidong Liu will coordinate actions on the code issues list and report back at the 4Q05 meeting. Colin will chair this team.

10. FSA Checklist

See presentation from Ken Brock (Silvaco) on the CMC website.

Members can contact Ken if they want to get involved in future efforts.

11. BSIM3/BSIM4/BSIM-SOI (Jane Xi)

See Jane's slides on website.

12. Resistor Model Subcommittee (Colin McAndrew – Freescale)

See presentation slides for details.

Members in attendance voted unanimously to adopt the R2 model as a standard.

13. Membership Matters (All)

Mark Basel (Mentor) presented on non-ideal FET geometries. See website for presentation details.

Members can contact Mark for further discussion on this topic.

#### 14. Next Meeting

The next meeting will be held on December 8 in Washington, DC.

Meeting topics will include next generation MOSFET model standard ballot results and next steps, budget discussion, and model code open issues.

Meeting Adjourned.

This meeting was conducted in accordance with the EIA Legal Guides and EIA Manual of Organization and Procedure.