

GEIA CMC 10/12/2006 MEETING MINUTES

Time: 7:00AM-5:00PM

Date: October 12, 2006

Place: MECC, Maastricht, The Netherlands

Note: details of information presented are not provided here, the presentations are posted on the CMC web site.

Joe Watts opened the meeting and introduced Evolvable Software, LSI Logic, and Sony as a new members.

Joe Watts reviewed the Agenda and expectations for outcomes of items for the day.

As one item is how to spend the remaining CMC funds for 2006, James Victory presented a summary of the MOS Varactor subcommittee. This included a proposal for funding of \$25K for 2006 and 2007 for ASU to pick up support for the varactor model.

Joe Watts reviewed the budget for 2006. The expectation is that there are 36.5 member companies. Joe also noted some companies have not yet paid, and dues were due at the end of June. For 2007 dues are due at the end of March. There is about \$60K available to spend still, proposals include \$25K for ASU for MOS varactor model support, distributing all or some to the supported Universities, and/or fund speed improvement for PSP. It was also proposed that instead of \$25K each in 2006 and 2007 that there could be one payment of \$50K for 2007. A line item will be added to the 2007 budget for LDMOS funding. A line item will also be added for MOS varactor model support to the 2007 budget.

AA: The officers will review the proposals for spending remaining funds. This will be circulated to all members to evaluate the proposal for funding for MOS varactor support and alternatives for 2006 and the 2007 proposed budget and come to the 4Q meeting prepared to vote on the proposal.

CMC EDA member companies reviewed the implementation status of standard models in their simulators (Cadence, Mentor Graphics, Synopsys, Agilent, Simucad, and Ansoft).

Question: Can Synopsys provide a modular model interface for Hspice?

AA: Can Synopsys to respond re modular model interface question at the 4Q meeting? (Note: the CMC does not control EDA member interfaces).

Anjan Chakravorty presented an updated on HiCUM. There was some discussion about the iterative bug fixes to the model; Joe Watts noted that the CMC has defined a model release and QA procedure. This has perhaps not included the model developers in the definition and application procedure as much as it should.

AA: Model release and QA procedures should be communicated again, and model developers engaged in the process. Colin can help people get going (Anjan for HiCUM).

Slobodan Mihalkovic presented an update on Mextram. Slobodan proposed adding a Verilog-A revision number to the "release" number. This was not accepted. Slobodan proposed model updates for version 504.6.2 at the end of October, this was agreed to. He also proposed updates for a sub-version 504.7.0 release in December 2006: EB tunneling and lbc splitting were the main items. Ramses van der Toorn (NXP) noted that the lbc splitting interacts with the epi model in Mextram and should be looked into more, Doug Weiser (TI) commented that the lbc would be good for their technologies. Slobodan also noted a geometry scalable code is available in Verilog-A, and TU Delft are also working on a sectionalized model. The Mextram Users Group and Verilog-A code releases are to be split, the latter will be on SourceForge

(<http://sourceforge.net/projects/mextram>). The CMC was not interested in standardizing the scaling relations for Mextram.

AA: TI will provide data to TU Delft on the Ibc diode currents, and NXP and TU Delft will investigate further the need for this and the physical formulation; the tunneling current will be included in the next beta release.

Dick Klaassen (NXP) has been the primary CMC representative, many of his colleagues have not attended meetings before but did as it was convenient at the meeting in Maastricht, so Dick introduced his NXP (and former NXP) colleagues. Ramses van der Toorn reviewed the Mextram 3500 model, for GaAs HBTs. Non-ideality factors were added to currents, and the major changes were in modeling of the collector depletion charge. There was some interest in this as a standard model; it was asked if it could be merged in with Mextram 504. Agilent noted that they had also recently released an HBT model.

AA: Mextram 3500/NXP will present position on making available publically at 4Q meeting. Agilent will present on their HBT model at the 4Q meeting. CMC (Joe Watts) will look to invite other companies and people interested in III-V HBT models to attend the 4Q meeting.

Takahiro Iizuka (NEC) presented features of the HiSIM-LDMOS model. There was a request for data from companies for comparison/verification; the CMC process was for interested companies to fit the models to their own data independently, rather than provide standard data sets, because of the wide range of device structures.

Linda Smith (National Semiconductor) presented a report from the LDMOS subcommittee. MM21 has been given some evaluation, EKV-HV will present at the December meeting.

STARC noted they had not received e-mail re the LDMOS subcommittee meetings. There was some discussion that the subcommittee mailings are not general as they sometimes can be frequent and contain very detailed data. It would be nice to have self-subscribing e-mail lists.

AA: Keith Green will investigate with the GEIA about having mail lists for the subcommittees set up so that people can subscribe or unsubscribe, without having to have this managed manually by the subcommittee chair.

AA: ? Should new members be given a package that includes details of how the subcommittees (and other procedures) work.

Annemarie Aarts presented a review of MM20. ADI (Geoffrey Coram) can provide MM20 2002.2 Verilog-A with self-heating. NXP will run this against their tests to verify the implementation (and work with ADI on ensuring what version of the model is used and what effects are in it, e.g. quasi-saturation).

Joe reviewed the CMC web site updates, from Keith Green. A wiki-type capability is being added by the GEIA and should be available by the end of 2006.

Joe reviewed the proposed CMC policy on standard names. It was generally agreed to. Non-standard parameters will begin with "ncmc_" as a prefix. Also "CMC Compliant Implementation" and "CMC Standard Parameter Set" shall be the terms that are applied. The first "May" will be changed to "Must." The naming policy was agreed to be adopted. Ivan recommended an official GEIA press release that states the new policy; this was agreed to.

Dick Klaassen (NXP) provided an update on the status of PSP. This included a description of the PSP102.1 model. This will be released in C code (NQS) and Verilog-A in the SiMKit 2.4 by the end of October. This release was agreed to by the CMC members in attendance. New research developments under development were also reviewed. These included: a vertical doping

uniformity model, PSP-SOI-PD (will be presented to the CMC for evaluation and consideration for standardization in the future, when ready), EVB tunneling, a preliminary body resistance model, a dynamic depletion (DD) model for general SOI.

Joachim Assenmacher (Infineon) presented proposals for PSP102 enhancements.

AA: PSP102.1 code to be released on the PSP webs site by October 31, 2006.

Priority items were listed, and discussed for need and status/effort.

Proposed items to consider for updates:

1. Add dielectric constant as a parameter
2. Add instance parameters DELVT0 and FACTU0
3. Improve effective doping model (lateral)
4. Add substrate resistance network
5. Add support for NF
6. Add separate junction parameters for source and drain
7. Add Rg (and Rsub) for QS model (switch for effects separately)
8. Nonuniform vertical doping
9. Consistency of IV and CV for pocket implant model
10. Thermal node added (including self-heating)
11. Temperature behavior of capacitance, wrong qualitative behavior (also for MOS varactor)
12. Archaic syntax and hidden state issue (fixed in PSP102.1)
13. CJSWG issue, capacitance changes with gate bias
14. Simulation time reduction

Evaluation of items:

1. (now) easy
2. (now) easy
3. (near future) needs investigation (priority)
4. (future) VA issue
5. (now) tedious, exactly define (BSIM4.xx ?; WPE and STI)
6. (now) tedious
7. (future) VA issue
8. (future) at present being researched (priority)
9. (future) Needs definition and data
10. (???) infrastructure issue
11. (near future) needs some investigation
12. (now) done
13. (future) needs research
14. (on-going)

AA: Close on PSP priority list via e-mail, work with ASU/NXP on feasibility etc.

Chung-Hsun Lin presented a status update on the BSIM family of models.

AA: Joe to check with AMD whether they need the K1ox updated to BSIM-SOI3.2.

Colin presented the status of the Verilog-A test suite from Tiburon. It has been placed on the CMC web site and is available for testing. There has been little feedback (ADI, Cadence, Freescale).

AA: All interested parties need to test and provide feedback to Tiburon, final release and acceptance will be in December.

Doug Weiser reviewed the QA subcommittee activities.

Colin McAndrew reviewed the resistor subcommittee activities.

Joe Watts reviewed the standard model file format subcommittee with slides from Geoffrey Coram.

Paul Humphries reviewed the proximity subcommittee activities.

AA: All subcommittees to continue activities and report at the 4Q meeting, all CMC members to appropriately participate in subcommittees.

Joe Watts reviewed the action items from the previous meeting.

The next meeting we will try for 1.5 days (Thu. and Fri. AM, to allow people, especially international travelers, to leave Fri. PM) or 2.0 days (Thu. and all of Fri.).

Paul Humphries commented that in the NXP documentation it can be difficult to work out what a quantity is (parameter etc.). Documentation will be discussed at the 4Q2006 meeting.

Joe Watts closed the meeting.

Members attending:

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|----------------|-----------|
| Tinti | Roberto |
| Humphries | Paul |
| Mertens | Samuel |
| Kraus | Wolfgang |
| Belousov | Alexander |
| Baystryuk | Sergey |
| Takada | Yorio |
| Kosukegawa | Tsutomu |
| Ito | Makoto |
| McAndrew | Colin |
| Watts | Josef |
| Assenmacher | Joachim |
| Victory | James |
| Liu | William |
| Harker | Shane |
| Yamaguchi | Tad |
| Smith | Linda |
| Iizuka | Takahiro |
| Klaassen | Dirk |
| Scholten | Andries |
| van der Torm | Ramses |
| van Langevelde | Ronald |
| Driessen | Marjan |
| Smit | Gert-Jan |
| Lee | Peter |
| Kolev | Plamen |
| Pesic | Ivan |
| Warwick | Chris |
| Chihiro | Arai |
| Furui | Yoshiharu |
| Inakagi | R. |
| Juge | André |
| Celi | Didier |
| Kauffman | Nicolas |
| Weiser | Doug |
| Kawakita | Hideyuki |
| Mishori | Boris |

Non-Members attending:

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|-------------|------------|
| Wu | H.-C. |
| Mijalkovic | Slobodan |
| Milovanovic | Vladimir |
| Lin | Chung-Hsun |
| Schroter | Michael |
| Chakravorty | Anjan |
| Gneiting | Thomas |
| Aarts | Annemarie |

Member Companies Absent:

**Agere Systems
AMD
Broadcom
Cypress Semiconductor
Intel
Intersil
LSI Logic
Mentor Graphics
Samsung
Sandia National Laboratories
SRC
Synopsys, Inc
TSMC
United Microelectronics Corporation**

Voting rights status:

Companies with **ACTIVE** voting status:

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| <p>Agere Systems Agilent Technologies Analog Devices Ansoft Corporation Atmel Broadcom Cadence Design Systems Cypress Semiconductor Freescale Semiconductor IBM Infineon Intel Intersil Jazz Semiconductor Maxim Mentor Graphics National Semiconductor NEC Electronics NXP Renesas Technology Corporation RF Micro Devices Simucad STARC ST Microelectronics Synopsys, Inc Texas Instruments Toshiba Corporation Tower United Microelectronics Corporation</p> |
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Companies with **INACTIVE** voting status:

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| <p>AMD Elpida Evolvable Systems Research Institute LSI Logic Samsung Sandia National Laboratories Sony SRC TSMC</p> |
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