



BSIM Update

BSIM Group

University of California, Berkeley

Compact Modeling Council Meeting, Dec. 15, 2006



BSIM4.6.0 Release

Model Release

- BSIM4.6.0 model released on 12/13/2006
- The release contains the following features
 - Asymmetric leakage modules
 - separated Gate Induced Source Leakage (GISL) parameter sets
 - separated Gate Edge Drain Leakage (GEDL) parameter sets
 - separated Gate Overlap source-side current parameter sets
 - Columbic scattering module in mobility model
 - Improvement to NOIMOD=2
 - In accordance with CMC QA requirements, BSIM4.6.0 model parameters and corresponding QA test results.

GISL / GIDL Leakage Module

- In BSIM 4.5.0, both I_{GISL} and I_{GIDL} share the same set of parameters – AGIDL, BGIDL, CGIDL and EGIDL.
- In BSIM 4.6.0, the parameters for I_{GISL} and I_{GIDL} are different.
- 4 new parameters – AGISL, BGISL, CGISL and EGISL and the corresponding L, W and P binning parameters have been added.

$$I_{GIDL} = AGIDL \cdot W_{effCJ} \cdot Nf \cdot \frac{V_{ds} - V_{gse} - EGIDL}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL}\right) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3}$$

$$I_{GISL} = AGISL \cdot W_{effCJ} \cdot Nf \cdot \frac{-V_{ds} - V_{gde} - EGISL}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGISL}{-V_{ds} - V_{gde} - EGISL}\right) \cdot \frac{V_{sb}^3}{CGISL + V_{sb}^3}$$

- Backward compatibility with BSIM4.5.0 maintained.

Junction Diode I-V

- In BSIM4.6.0, the parameters for source and drain side junction diode current due to the trap-assisted tunneling current in space-charge region have been separated.
- 6 new parameters are added for the drain side.
 - NJTSD, NJTSSWD, NJTSSWGD, TNJTSD, TNJTSSWD, TNJTSSWGD

$$I_{bd_total} = I_{bd}$$

$$-W_{effj} \cdot NF \cdot J_{tsswgd}(T) \cdot \left[\exp\left(\frac{-V_{bd}}{NJTSSWGD(T) \cdot Vtm0} \cdot \frac{VTSSWGD}{VTSSWGD - V_{bd}} \right) - 1 \right]$$

$$NJTSD(T) = NJTSD(TNOM) \cdot \left[1 + TNTJSD \left(\frac{T}{TNOM} - 1 \right) \right]$$

$$-P_{d,deff} J_{tsswd}(T) \cdot \left[\exp\left(\frac{-V_{bd}}{NJTSSWD(T) \cdot Vtm0} \cdot \frac{VTSSWD}{VTSSWD - V_{bd}} \right) - 1 \right]$$

$$NJTSSWD(T) = NJTSSWD(TNOM) \cdot \left[1 + TNJTSSWD \left(\frac{T}{TNOM} - 1 \right) \right]$$

$$-A_{d,deff} J_{tsd}(T) \cdot \left[\exp\left(\frac{-V_{bd}}{NJTSD(T) \cdot Vtm0} \cdot \frac{VTSD}{VTSD - V_{bd}} \right) - 1 \right] + g_{\min} \cdot V_{bd}$$

$$NJTSSWGD(T) = NJTSSWGD(TNOM) \cdot \left[1 + TNJTSSWGD \left(\frac{T}{TNOM} - 1 \right) \right]$$

Gate Tunneling Current I_{GS} / I_{GD}

- In BSIM4.6.0, gate tunneling currents in the overlapping S/D diffusion regions, I_{GS} and I_{GD} , have different set of parameters.
- The new parameters for I_{GS} and I_{GD} are :
 - I_{GS} : DLCIG, AIGS, BIGS, CIGS
 - I_{GD} : DLCIGD, AIGD, BIGD, CIGD
 - L, W and P binning parameters for AIGS, BIGS, CIGS , AIGD, BIGD, CIGD.

$$I_{gs} = W_{eff} DLCIG \cdot A \cdot T_{oxRatioEdge} \cdot V_{gs} \cdot V_{gs}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot (AIGS - BIGS \cdot V_{gs}') \cdot (1 + CIGS \cdot V_{gs}')\right]$$

$$I_{gd} = W_{eff} DLCIGD \cdot A \cdot T_{oxRatioEdge} \cdot V_{gd} \cdot V_{gd}' \cdot \exp\left[-B \cdot TOXE \cdot POXEDGE \cdot (AIGD - BIGD \cdot V_{gd}') \cdot (1 + CIGD \cdot V_{gd}')\right]$$

- The parameters from BSIM4.5.0 are retained for backward compatibility.

Coulomb Scattering Mobility Model

- The coulomb scattering term has been modified in BSIM4.6.0 release to avoid the possibility of non-monotonic drain current trend with respect to gate voltage. [Reported by ADI]

mobMod=0

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC V_{bseff}) \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right)^2 + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}} \right)^2}$$

mobMod=1

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left[\frac{V_{gsteff} + C_0 \cdot (V_{THO} - V_{FB} - \Phi_s)}{TOXE} \right]^{EU} + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}} \right)^2}$$

mobMod=2

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + \left[UA \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right)^2 \right] (1 + UC \cdot V_{bseff}) + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}} \right)^2}$$

Improvement to NOIMOD = 2

- In b4noi.c, replace the noise resistance R_{geltd} by the following resistor [Reported by Mentor Graphics]

$$R_{geltd} \times \left(1 + \frac{R_{ii}}{R_{geltd}} \right)^2$$

- Note that the change in NOIMOD=2 in BSIM4.6.0 is backward incompatible with BSIM4.5.0.
- Change the code in b4noi.c. (red is deletion, blue is addition)

```
if ((here->BSIM4rgateMod == 1) || (here->BSIM4rgateMod == 2))
    { NevalSrc(&noizDens[BSIM4RGNOIZ],
              &lnNdens[BSIM4RGNOIZ], ckt, THERMNOISE,
              here->BSIM4gNodePrime, here->BSIM4gNodeExt,
              here->BSIM4grgeltd);
    }
else if (here->BSIM4rgateMod == 2)
    {
    T0 = 1.0 + here->BSIM4grgeltd/here->BSIM4gcrg;
    T1 = T0 * T0;
    NevalSrc(&noizDens[BSIM4RGNOIZ],
              &lnNdens[BSIM4RGNOIZ], ckt, THERMNOISE,
              here->BSIM4gNodePrime, here->BSIM4gNodeExt,
              here->BSIM4grgeltd/T1);
    }
```

Bug Fix : b4set.c

- The model parameter VFB was not initialized in BSIM4.5.0.
- b4set.c has been modified to initialize VFB parameter.
- The following lines have been added to the code in b4set.c :

```
if (!model->BSIM4vfbGiven)  
    model->BSIM4vfb = -1.0;
```

Changes to Manual

- The relevant chapters in the manual have been updated (Ch-4, 5, 6, 10, 12).
- Impact Ionization parameter list in Appendix-A has been updated to reflect the correct model parameters. The model equation in Ch-6 has also been corrected.
- The guidelines for extracting the Well proximity model parameters (Ch-14) have been removed and reference to the CMC WPE parameter extraction document has been provided.



BSIMSOI 4.1 beta Release

BSIMSOI4.1 beta Release

- BSIMSOI4.1 beta model will be released at end of this month
- The release contains the following enhancement
 - New model parameters: gate dielectric constant (EPSROX), flat band voltage (VFB)
 - Asymmetric GIDL/GISL module
 - Improved charge model of body contacted device
 - bug fixes over BSIMSOI4.0

Gate Dielectric Constant

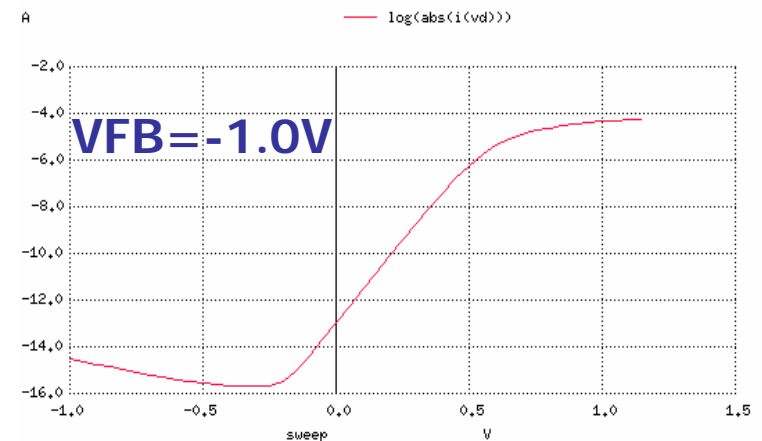
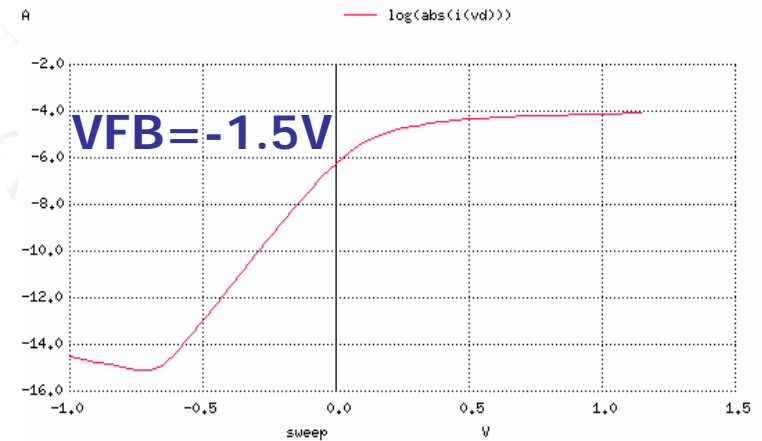
■ EPSROX

- Replace EPSOX (or $3.453133e-11$) with $EPSROX * 3.453133e-11 / 3.9$
- In *lit* calculation, replace $3 * Xdep * tox$ with $EPSROX / 3.9 * 3 * Xdep * tox$
- In GIDL/GISL calculation, replace $(Vdg - EGIDL) / (3 * tox)$ with $(Vdg - EGIDL) / (EPSROX / 3.9 * 3 * tox)$
- The default value of EPSROX is 3.9 for backward compatibility.

Flat Band Voltage

■ VFB

- Introduce VFB parameter for devices with tunable gate work function material
- If V_{th0} is not given, then V_{th0} is calculated from $VFB + \phi_{is} + K1*\sqrt{\phi_{is}-V_{bs}}$
- The default value of VFB is -1.0 for backward compatibility.
- Additional three binning parameters: LVFB, WVFB, PVFB



Asymmetric GIDL/GISL module

- In BSIMSOI4.0, I_{GISL} is not modeled.
- In BSIMSOI4.1, I_{GISL} is modeled using model parameter set different from I_{GIDL}
- Implementation of independent source-side GISL:
 - 4 new parameters – AGISL, BGISL, CGISL and EGISL and the corresponding L, W and P binning parameters have been added.

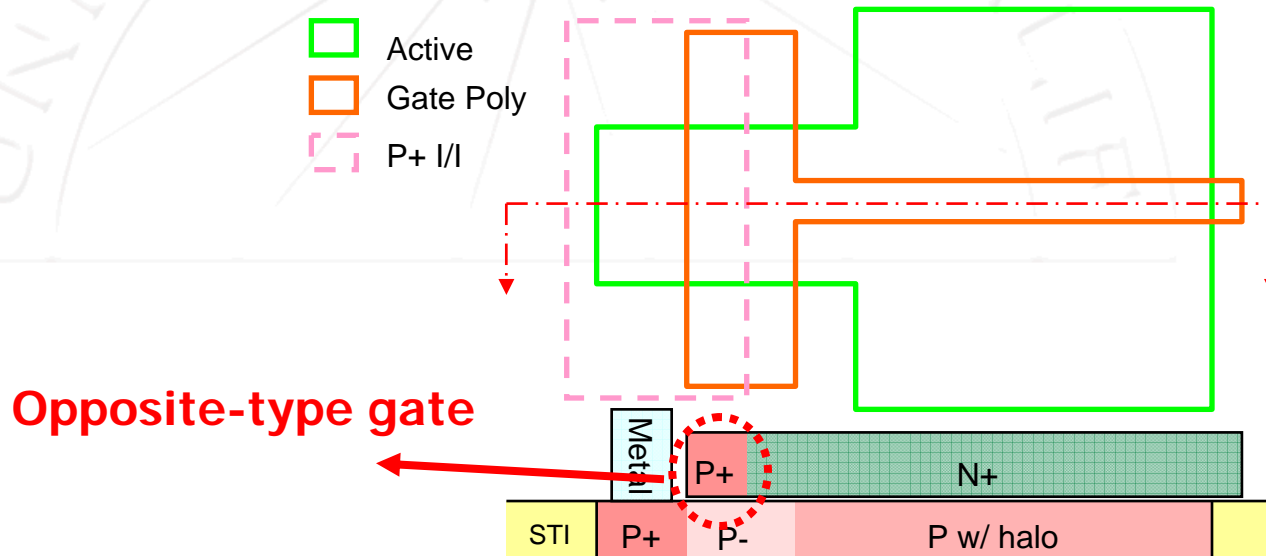
$$I_{GIDL} = AGIDL \cdot W_{effCJ} \cdot Nf \cdot \frac{V_{ds} - V_{gse} - EGIDL}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGIDL}{V_{ds} - V_{gse} - EGIDL}\right) \cdot \frac{V_{db}^3}{CGIDL + V_{db}^3}$$

$$I_{GISL} = AGISL \cdot W_{effCJ} \cdot Nf \cdot \frac{-V_{ds} - V_{gde} - EGISL}{3 \cdot T_{oxe}} \cdot \exp\left(-\frac{3 \cdot T_{oxe} \cdot BGISL}{-V_{ds} - V_{gde} - EGISL}\right) \cdot \frac{V_{sb}^3}{CGISL + V_{sb}^3}$$

- Backward compatibility with BSIMSOI4.0 maintained

C-V Model Improvement

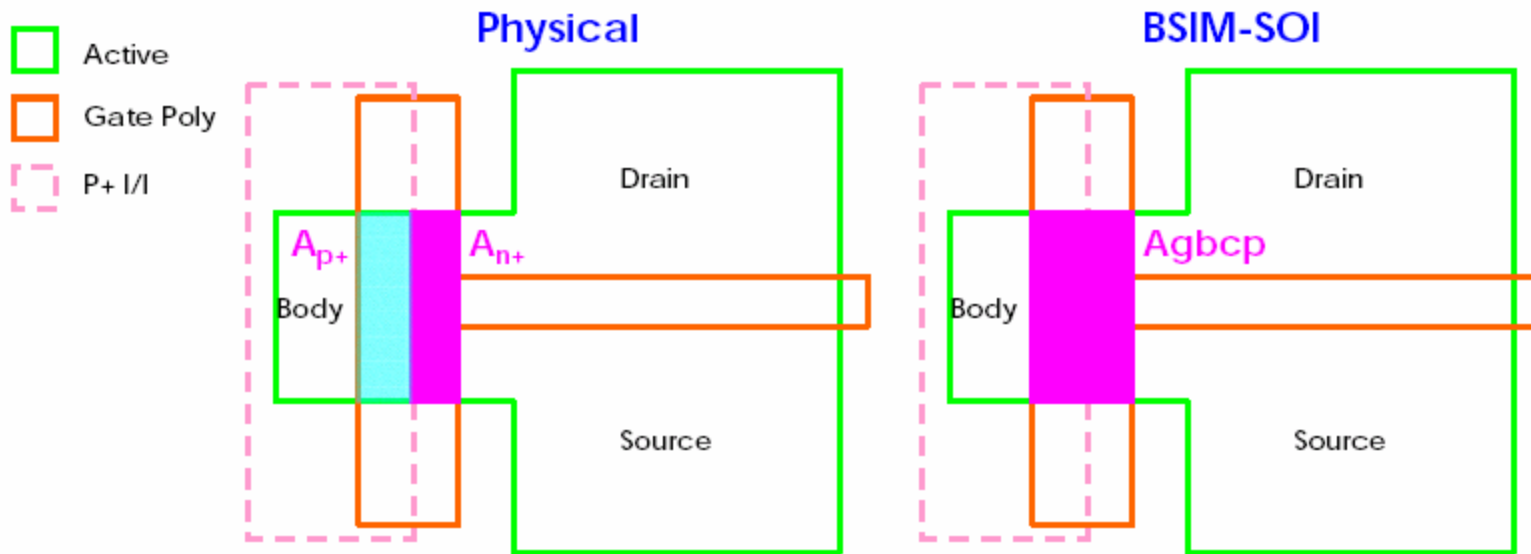
- Overestimation of gate charge in the body contact transistor due to opposite-type gate parasitic cap.
 - Reported by **Jung-Suk Goo, AMD**



Source: J.-S. Goo, MOS-AK 2005

- The P+ implantation for body contact will induce a parasitic P+-poly gate MOSCAP
- Charge on gate now consists of N+/P and P+/P- MOS-CAP.

Current BSIMSOI Capacitance Model

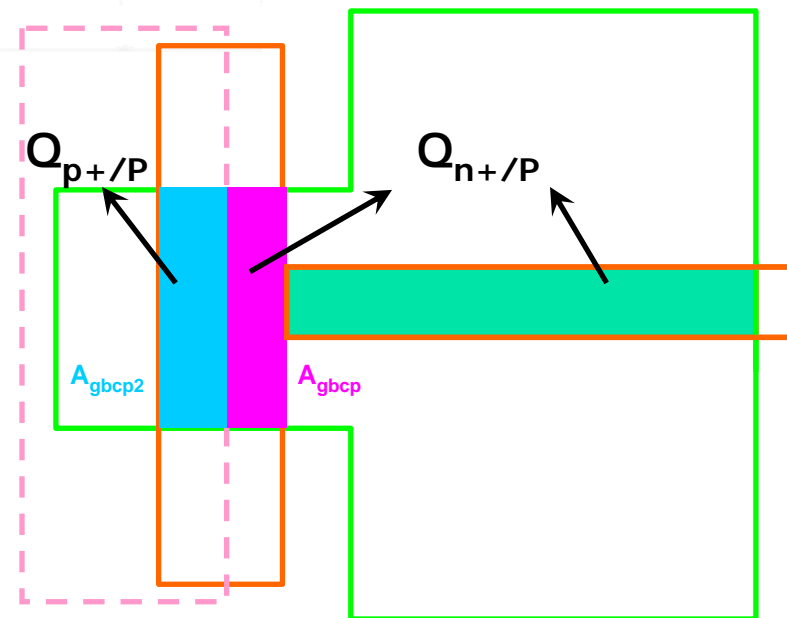


- In the current BSIMSOI model, the parasitic gate-to-body overlap due to body contact is modeled by one MOSCAP only (N+/P here)
- This leads to an overestimation of gate charge and hence larger delay in circuits.

Improved Charge Model

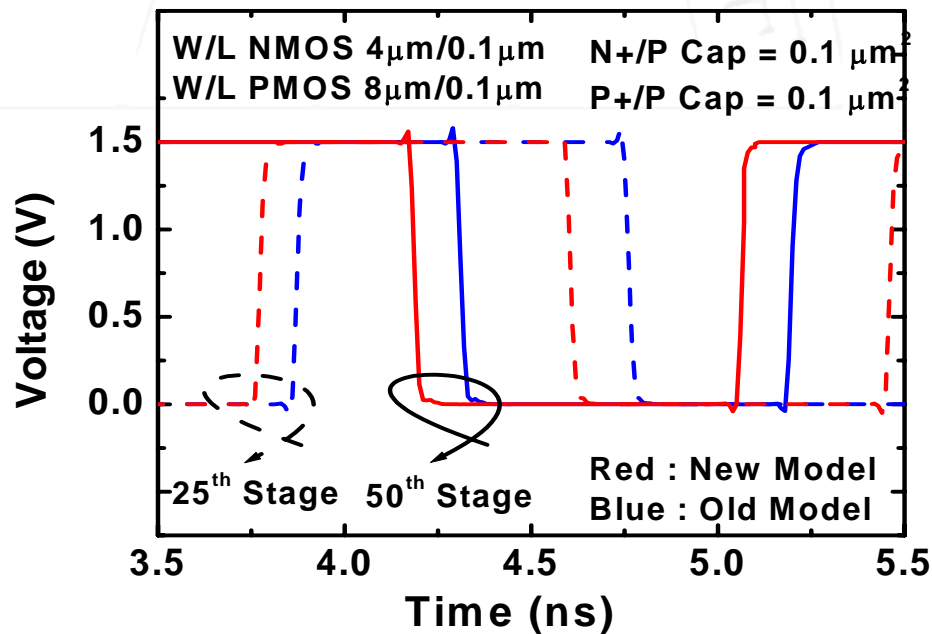
- Charge model modified to include the effect of p+/P region.
- Higher V_{FB} in the p+/P region lowers the gate charge and changes the C-V.
- Net gate charge is sum of n+/P region and p+/P region as shown below.
- One new model parameter **CR** to account for the non-ideal process variations
 - $A_{gbcp1} = A_{gbcp} * CR$
 - $A_{gbcp2} = A_{gbcp} * (1-CR)$

$$\begin{aligned}
 \text{Final charge} &= A_{gbcp1} \times n^+/\text{NMOS} \\
 &+ WL \times n^+/\text{NMOS} \\
 &+ A_{gbcp2} \times p^+/\text{NMOS}
 \end{aligned}$$



New Model Results

- 51- stage ring oscillator shows a smaller delay/stage (6%) due to lower capacitance.
- The accuracy of the SOI model for body contacted device has been enhanced.



Bug Fixes over BSIMSOI4.0

- Small value of Tcen will create NaNQ issue
 - Reported by [Richard Williams, Cal Bittner, IBM](#)
 - Suggested solution: add clamp at line 4750 on Tcen in b4soild.c

```
+4750          Tcen = pParam->B4SOIdeb - 0.5 * (V3 + V4);
+4751          T1 = 0.5 * (1.0 + V3 / V4);
+4752 // Tcen can underflow with right combination of tox, dtox, nch,
      bias
+4753          if (Tcen < 1e-15) {
+4754              Tcen = 1e-15;
+4755              T1 = 0;
+4756          }
```

Bugs Fixes over BSIMSOI4.0

- Vt equation for soiMod = 1,2 – FD subthreshold slope term
 - Reported by [Richard Williams, Cal Bittner, IBM](#)

- Bug:

+1422 T3 = pParam->B4SOIcdsc + pParam->B4SOIcdscb * **Vbseff**
+1423 + pParam->B4SOIcdscd * Vds;

Vbseff should be replaced by Vbs0mos

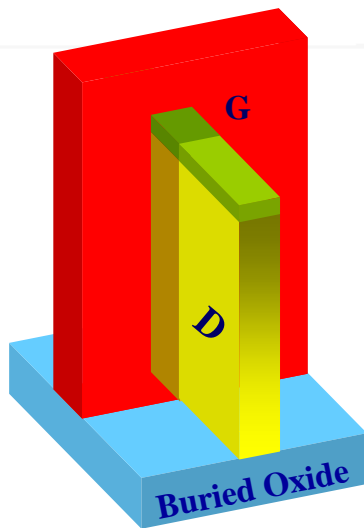
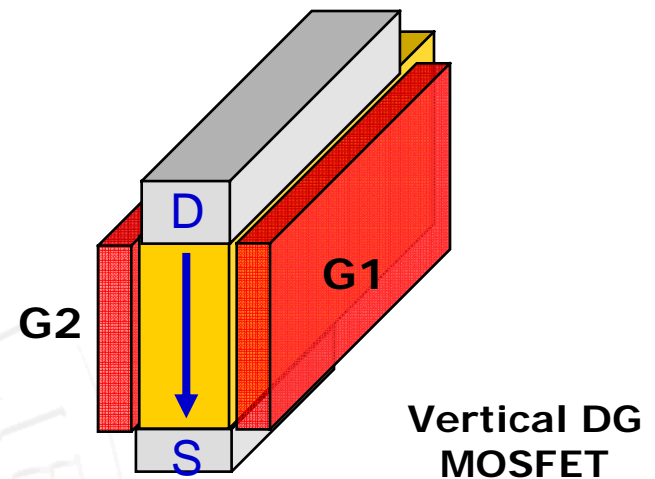
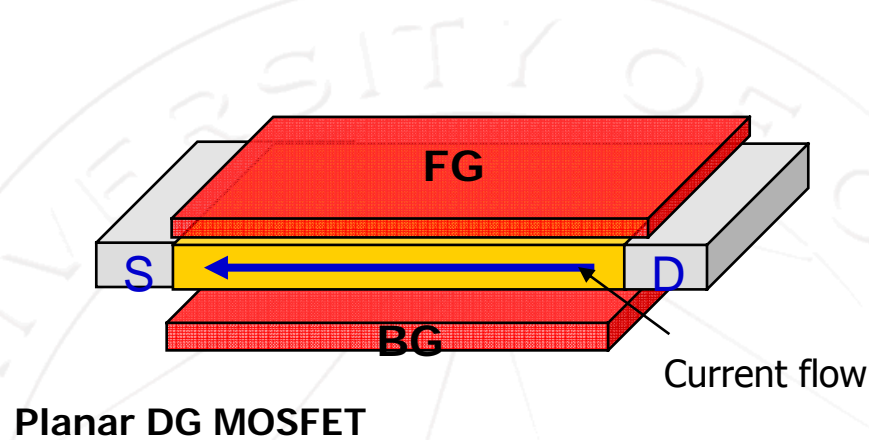
+1422 T3 = pParam->B4SOIcdsc + pParam->B4SOIcdscb * **Vbs0mos**
+1423 + pParam->B4SOIcdscd * Vds;

- Action: change b4soild.c accordingly
- Gate terminal charge (qgate) is added in debug=1 outputs for comparing simulators

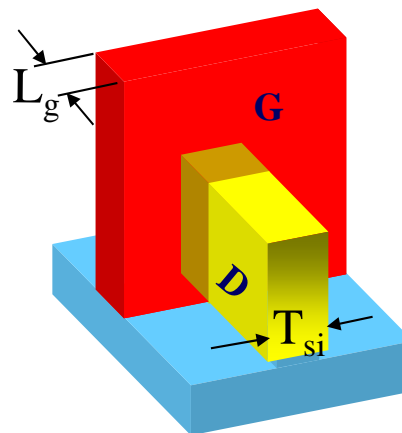


BSIMMG 1.0 alpha Release

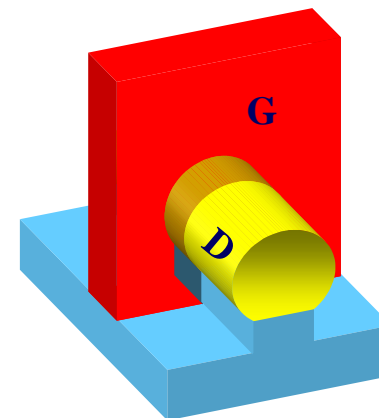
Versatile Multi-Gate Compact Model



Tall FinFET



Short FinFET
(Tri-Gate)



Nanowire FinFET
(Omega-Gate)

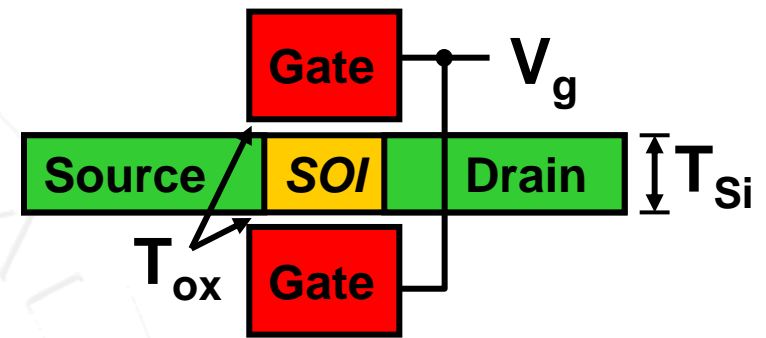
Symmetric Common-Gate Model

- “Symmetric” refers to the physical symmetry in the structure

- $T_{OX1} = T_{OX2} = T_{OX}$

- $V_{FB1} = V_{FB2} = V_{FB}$

- “Common” means that the two gates are always at the same voltage.



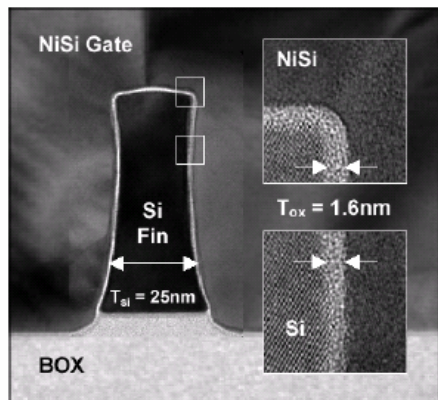
Symmetric Common DG-MOSFET

- The model is surface potential based.
- It can capture the effect of finite body doping on the electrical characteristics of MG-FET.
- Predictive and accurate core model without the use of any fitting parameter.

SOIMG and BulkMG Modules

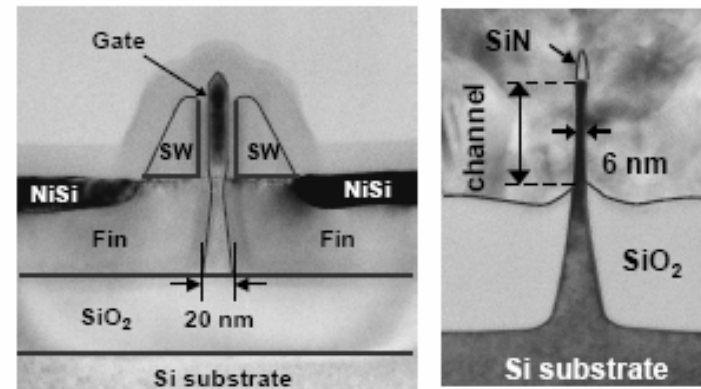
- Multi-gate transistor can be built on either Si substrate or SOI substrate

SOIMG



J. Kedzierski et al., IEDM 2002

BulkMG

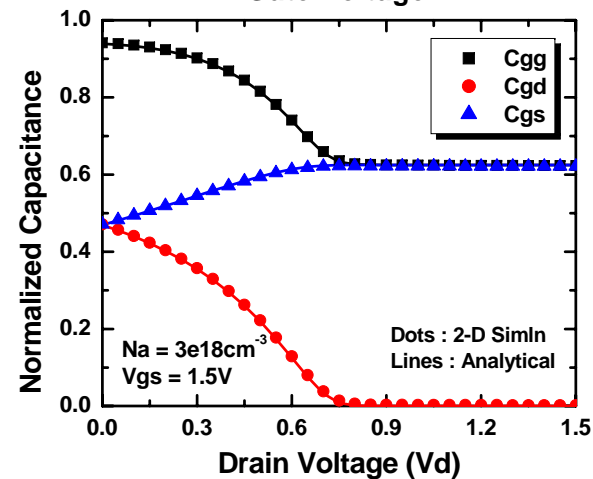
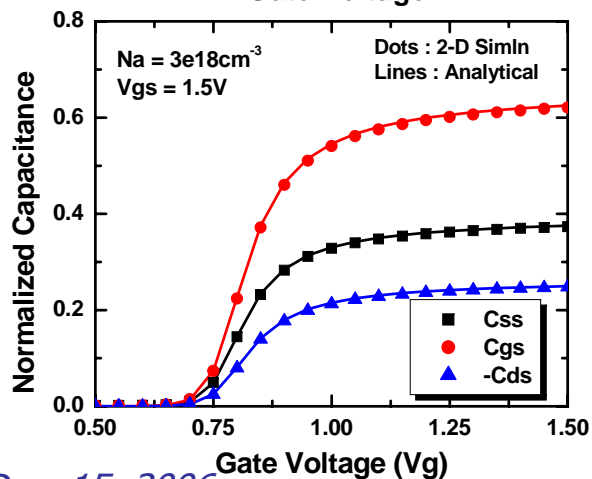
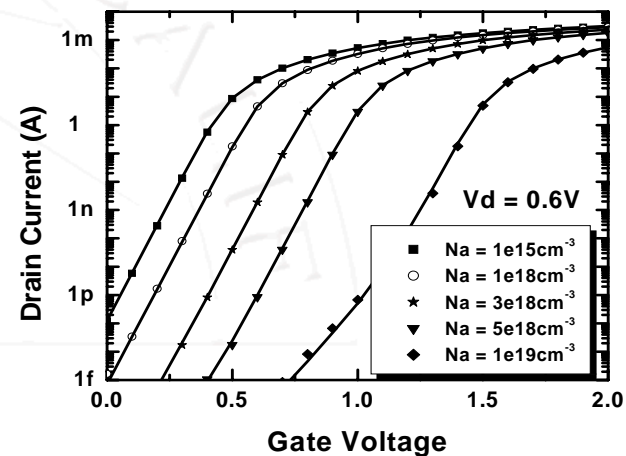
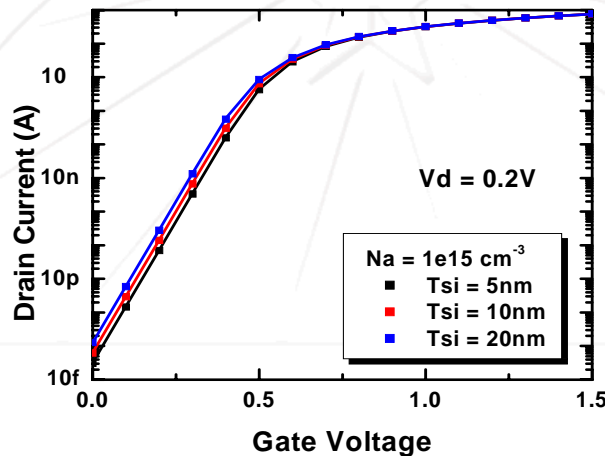


K. Okano et al., IEDM 2005

- BSIMMG1.0 alpha is implemented with two sub-modules: three-terminal SOIMG module and four-terminal BulkMG module

Core Model Verification with TCAD

- Model works well over a wide range of doping and various body thicknesses.
- Model is symmetric and continuous at $V_{ds}=0$

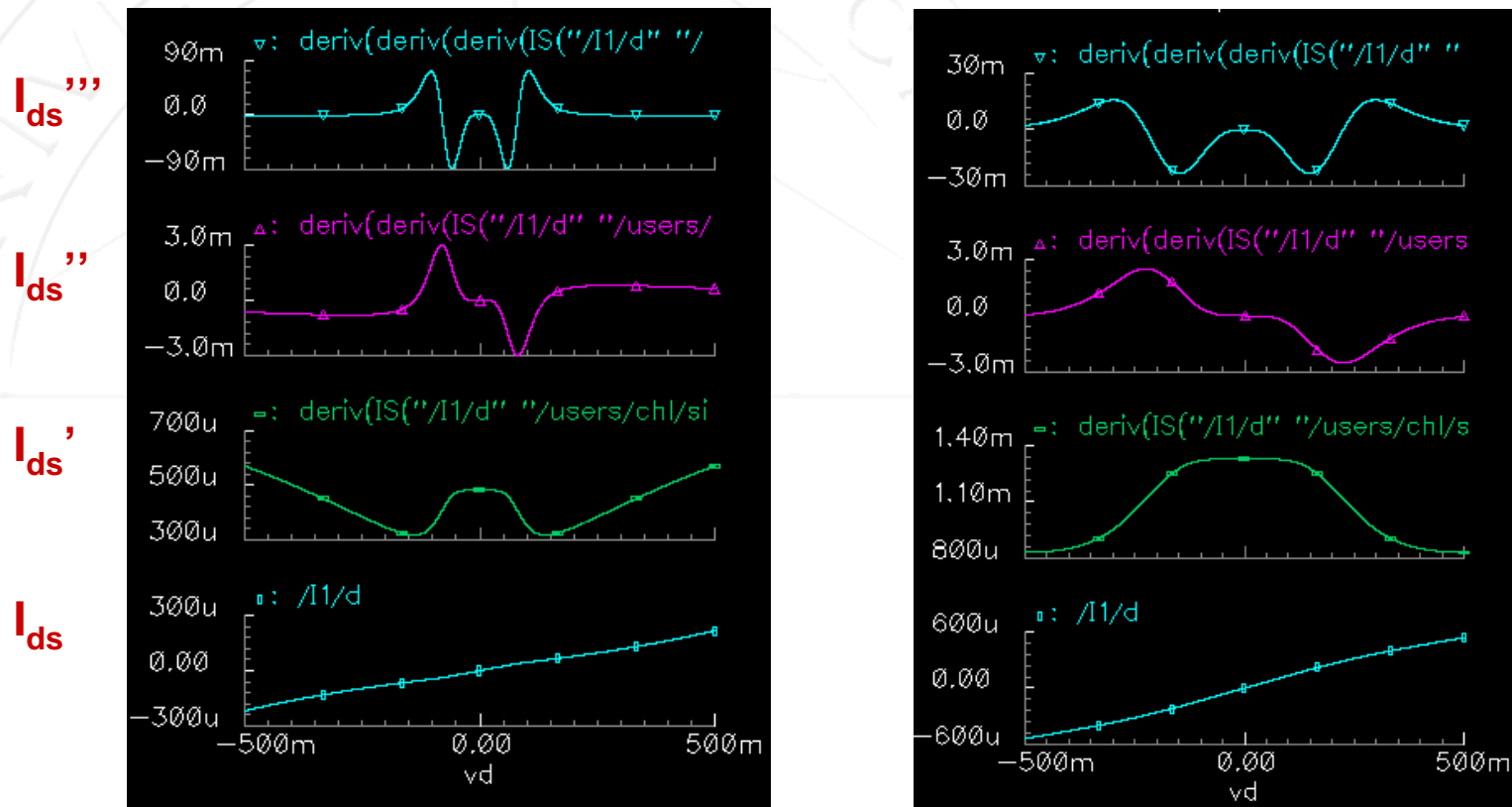


Modules in BSIMMG1.0 alpha

- Quantum Mechanical Correction
- Short Channel Effects
 - VT Roll-off
 - Subthreshold swing degradation
 - DIBL
- Polysilicon Depletion Effect
- S/D Series Resistance
- Mobility Degradation
- Velocity Saturation
- Channel Length Modulation
- Velocity overshoot / Source End Velocity Limit
- GIDL, GISL and Junction Leakage
- Gate Tunneling Current
- Parasitic Capacitance

Gummel Symmetry Test

- Model maintains symmetry after implementing second order effect.



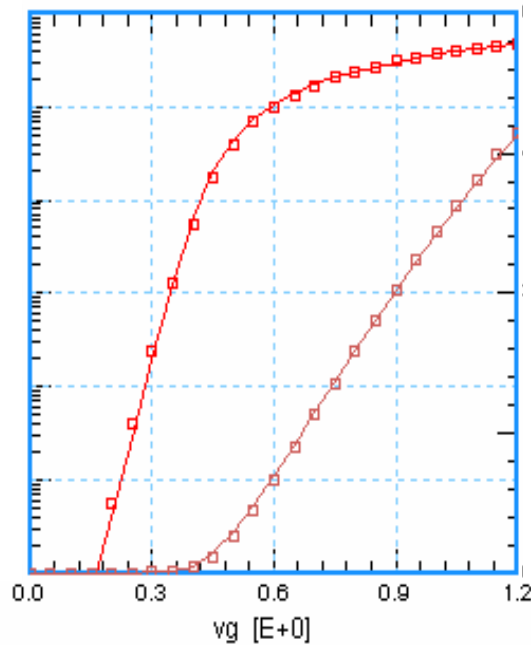
$V_g = 1V$

$V_g = 1.5V$

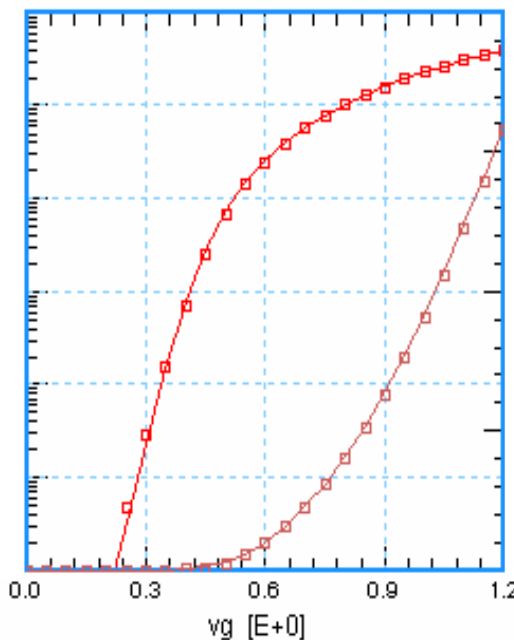
Fitting to Silicon

- BSIMMG1.0 alpha release is being used to fit the silicon data.
- Start from long channel device ($L_g=1\mu\text{m}$)
- Good fitting results (~ 10 parameters)

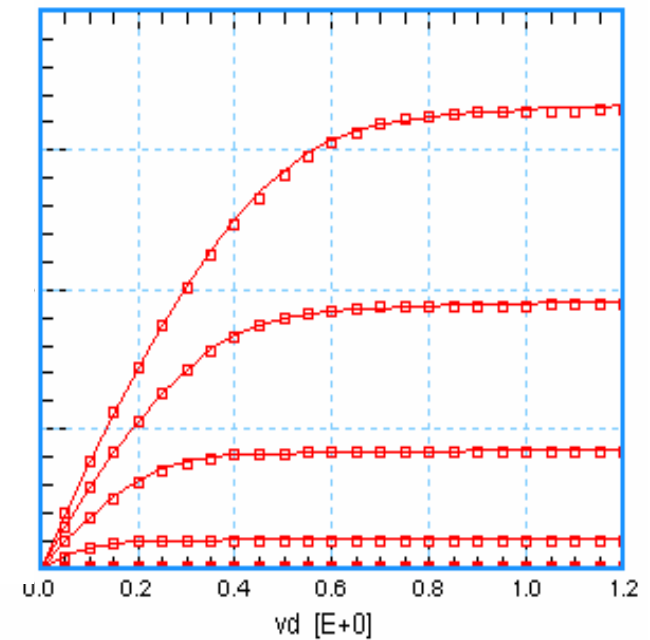
Ids-Vgs @ Vds=50mV



Ids-Vgs @ Vds=1.2V



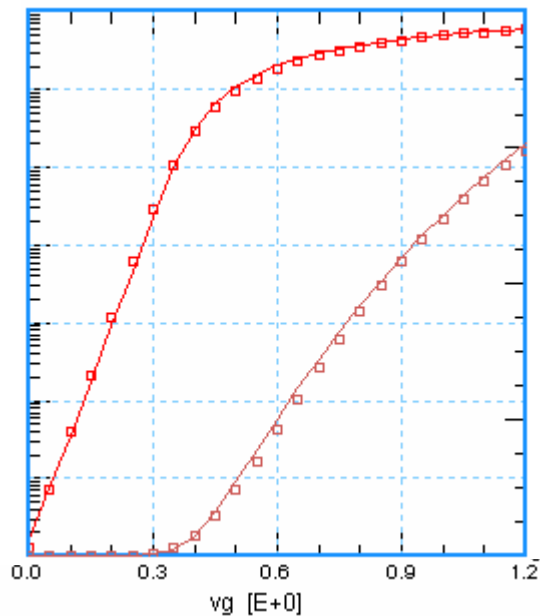
Ids-Vds @ Vgs=0-1.2V



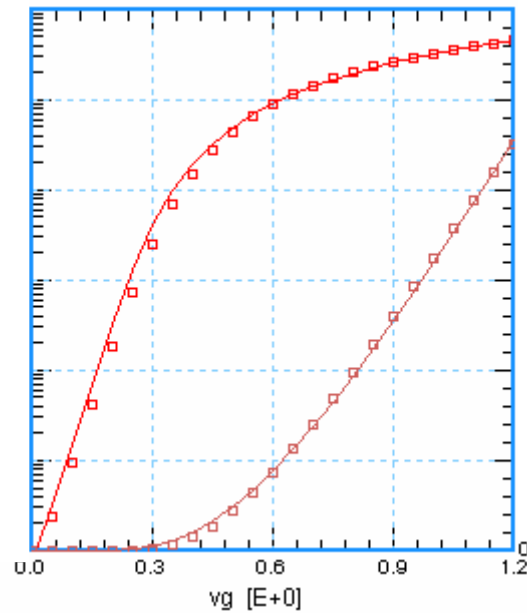
Fitting to Silicon

- Short channel device ($L_g=50\text{nm}$)
- Good fitting results

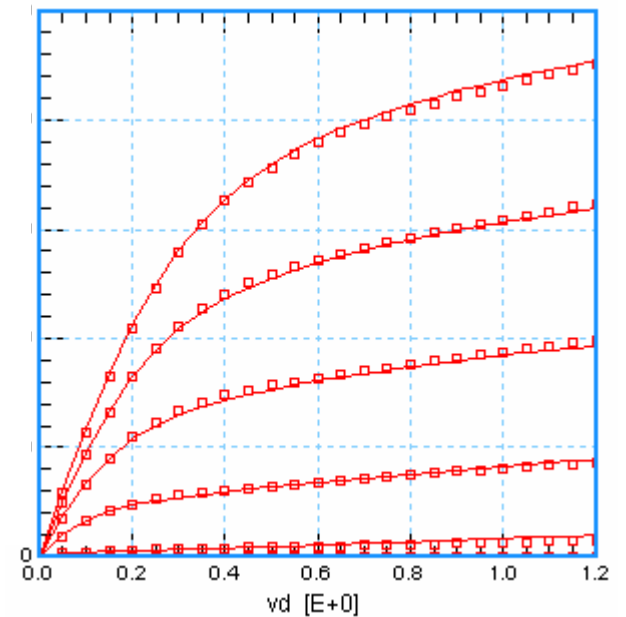
Ids-Vgs @ Vds=50mV



Ids-Vgs @ Vds=1.2V

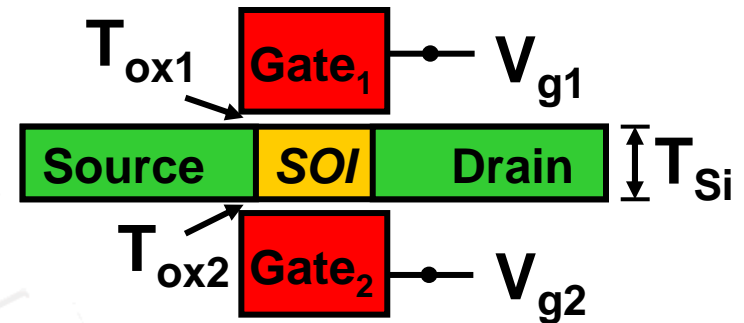


Ids-Vds @ Vgs=0-1.2V



Asymmetric Independent-Gate Model

- “Asymmetric” refers to the physical asymmetry in the structure
 - $T_{OX1} \neq T_{OX2}$
 - $V_{FB1} \neq V_{FB2}$
- “Independent” means that the two gates can be biased at different voltages.

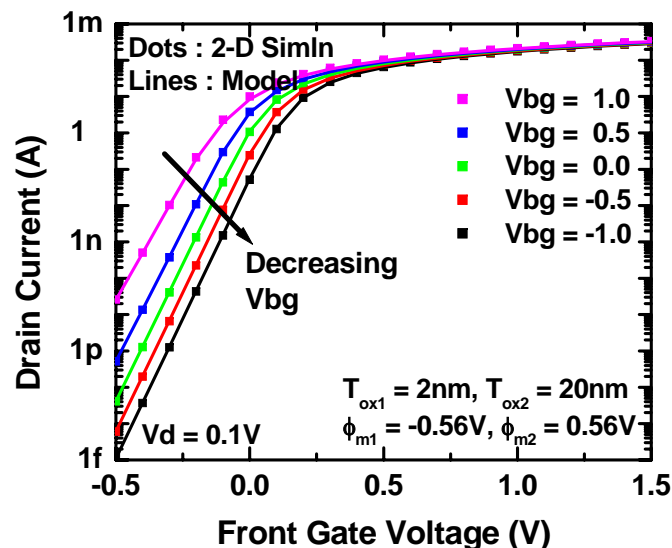
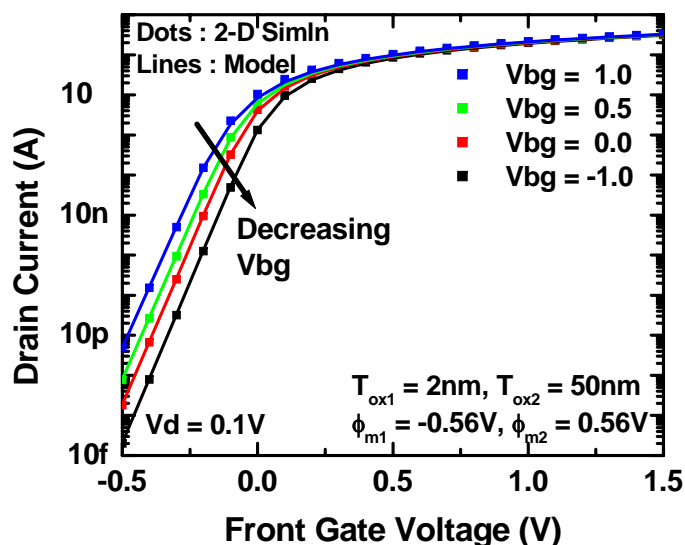
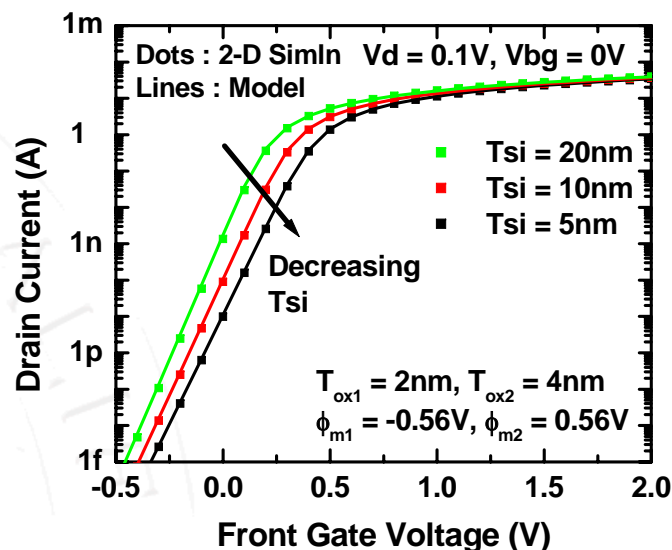


**Asymmetric Independent
DG-MOSFET**

- The model is surface potential based and assumes a lightly doped body.
- The model allows the presence of inversion channel at one surface only (a limit imposed on the C-V model, not the I-V).
- Predictive and accurate core model without the use of any fitting parameter.

I-V Model Verification

- Model is able to predict correct dependence of drain current on body thickness.
- The threshold voltage tuning by changing back gate bias is accurately predicted by the model.



BSIMMG1.0 alpha Version

- Symmetric Common MG-FET Mode
 - The α -version of this model has been released in October, 2006
 - Verilog-A code is available upon request
- Assymmetric Independent DG-FET Mode
 - The current goal is to release the α -version of this model by January, 2007

Summary

- **BSIM4.6.0 release**
 - Asymmetric leakage modules
 - Improved mobility model
 - Improved noise model
- **BSIMSOI4.1 beta release**
 - Gate dielectric constant
 - Flat band voltage
 - Asymmetric GIDL/GISL module
 - Improved charge model of body-contacted devices
- **BSIMMG1.0 alpha release**
 - Current version: symmetric common gate with doped channel
 - Asymmetric independent gate mode will be released early next year

Acknowledgement

- BSIM team would like to thank CMC members for the invaluable discussions and help with simulations

BSIM4.6.0:

- Claude Cirba (TI), David Zweidinger (TI), Yong Liu (TI), Keith Green (TI), Geoffery Coram (ADI), Colin McAndrew (Freescale)

BSIMSOI4.1 beta:

- Richard Williams (IBM), Cal Bittner (IBM), Judy An (AMD), Jung-Suk Goo (AMD), Qiang Chen (AMD), Weidong Liu (Synopsys)



Suggestions / Feedback?