

BSIM IMPROVEMENTS

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BSIM4 Improvements

Additional Leakage Modules (TI) - I

- Provided by TI.
- Leakage Module Enhancement from TI : GISL, GEDL, Gate overlap tunneling IV.
- Implementation of independent source-side Gate Induced Source Leakage:
 - Duplicate the current GIDL equation with new parameters to be applied to source
 - Restrict the current equation to drain-side only
 - Naming convention for source-side parameters: AGISL, BGISL, CGISL, EGISL
- If AGISL not given, then assume value of AGIDL
- Similarly for the other 3 parameters and the associated binning parameters.

Additional Leakage Modules (TI) - II

- Correction to the Gate Edge Source Leakage model for full source/drain separation:
- The GEDL model is only partially asymmetric, some parameters are common to source and drain side equations.
- Current common parameters that need to be separated drain/source:
 - NJTS, NJTSSW, NJTSSWG
 - TNJTS, TNJTSSW, TNJTSSWG
- New parameters: Adding D for drain association
 - NJTSD, NJTSSWD, NJTSSWGD
 - TNJTSD, TNJTSSWD, TNJTSSWGD
- If Drain parameter not defined, then assume the source value.

Additional Leakage Modules (TI) - III

- Implementation of independent Gate Overlap source-side current:
 - Separate the common gate overlap current equation into source/drain side
 - Current parameters that will be retained : DLCIG, AIGSD, BIGSD, CIGSD
 - New parameter for drain side : DLCIGD
 - New separate Drain and Source side parameters : AIGS, BIGS, CIGS, AIGD, BIGD, CIGD

- If DLCIGD not specified, take value of DLCIG.
- If AIGSD specified ignore AIGS/AIGD and set $AIGS = AIGD = AIGSD$.
- Activate the binning parameters (L,W,P)AIGSD only if AIGSD is given.
- Similar rules follow of BIGSD and CIGSD.

BSIM4.5.0 Mobility Model

- A new term was added in the mobility model to capture the Coulomb scattering effect in the BSIM4.5.0 release.

mobMod=0

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right)^2 + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2V_{th}} \right)^2}$$

mobMod=1

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + \left[UA \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right)^2 \right] (1 + UC \cdot V_{bseff}) + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2V_{th}} \right)^2}$$

mobMod=2

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left[\frac{V_{gsteff} + C_0 (V_{THO} - V_{FB} - \Phi_s)}{TOXE} \right]^{EU} + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2V_{th}} \right)^2}$$

Issue 1 : Backward Compatibility

- In BSIM4.5.0, the default value of the new parameter "UD" is 1e+14
- To have backward compatibility to BSIM 4.4.0 , UD should be explicitly specified to be zero in BSIM4.5.0 modelcards.
- To fix the issue, the default value of the new parameter "UD" is now set to 0.

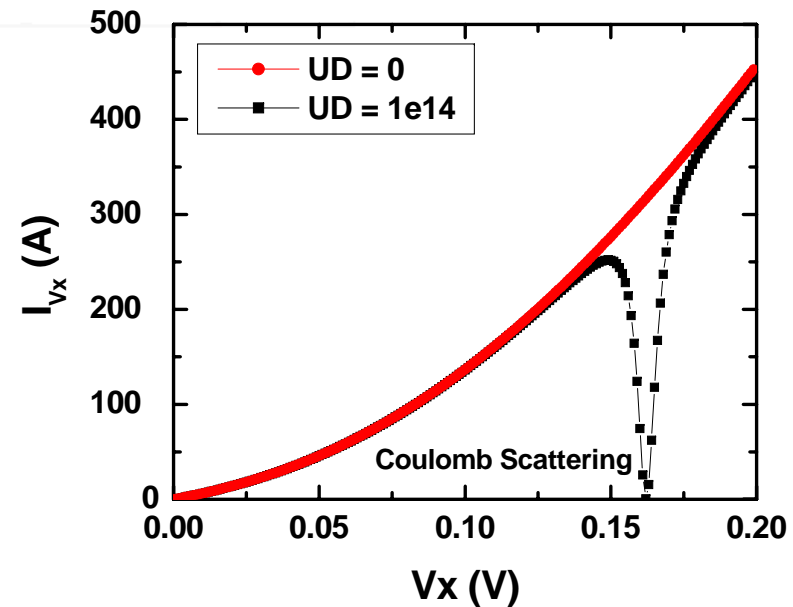
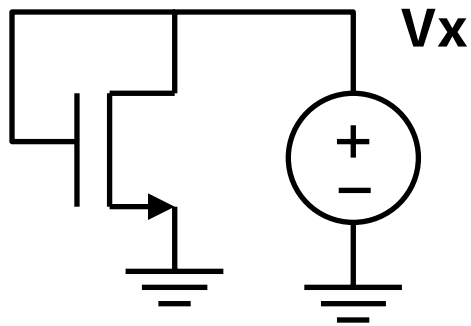
- For ex, for `mobMod = 0`,

NEW DEFAULT UD=0

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right)^2 + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2V_{th}} \right)^2}$$

Issue 2 : Non-Monotonic Drain Current

- Due to the new "UD" term, drain current can be non-monotonic in certain circumstances.
- If UD is explicitly set to 0, the problem is absent in BSIM4.5.0.
- If $V_{th} < 0$, $V_{gsteff} + V_{th}$ can approach zero and mobility can go to zero.



Model Correction

- Modify the coulomb scattering term for all mobMod's.

$$UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2V_{th}} \right)^2 \rightarrow UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}} \right)^2$$

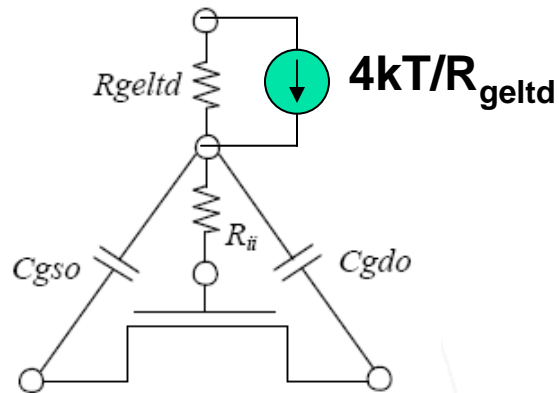
- In the new code, mobility model is (for ex: **mobMod = 1**)

$$\mu_{eff} = \frac{U0 \cdot f(L_{eff})}{1 + (UA + UC \cdot V_{bseff}) \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right) + UB \left(\frac{V_{gsteff} + 2V_{th}}{TOXE} \right)^2 + UD \left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.0001}} \right)^2}$$

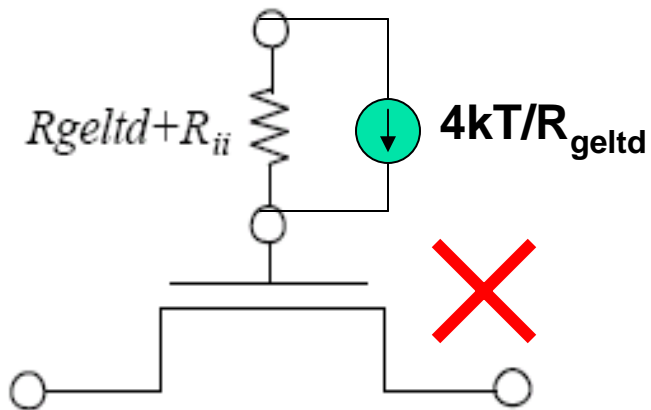
- Similarly change mobMod=2 and mobMod = 3

Error in NOIMOD = 2

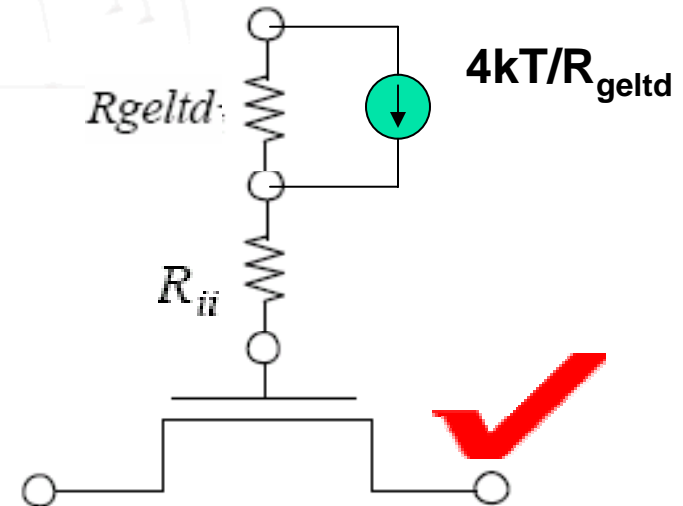
- When RgateMod = 3,



- When RgateMod = 2,



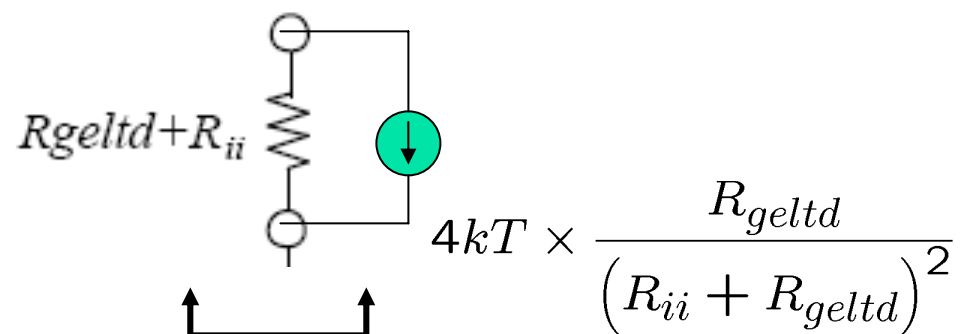
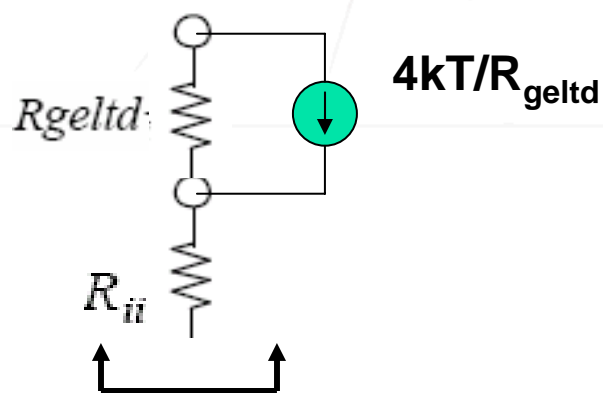
Current Model Implementation



CORRECT Model Implementation

Proposed Fix

- Model the noise by a current source with an “effective noise resistance” that gives correct noise.
- Correct Noise implementation:



New Model

- In b4noi.c, replace the noise resistance R_{geltd} by the following resistor

$$R_{geltd} \times \left(1 + \frac{R_{ii}}{R_{geltd}} \right)^2$$

- Change the code in b4noi.c.

```
if ((here->BSIM4rgateMod == 1) || (here->BSIM4rgateMod == 2))
    { NevalSrc(&noizDens[BSIM4RGNOIZ],
              &lnNdens[BSIM4RGNOIZ], ckt, THERMNOISE,
              here->BSIM4gNodePrime, here->BSIM4gNodeExt,
              here->BSIM4grgeltd);
    }
else if (here->BSIM4rgateMod == 2)
    {
    T0 = 1.0 + here->BSIM4grgeltd/here->BSIM4gcrg;
    T1 = T0 * T0;
    NevalSrc(&noizDens[BSIM4RGNOIZ],
              &lnNdens[BSIM4RGNOIZ], ckt, THERMNOISE,
              here->BSIM4gNodePrime, here->BSIM4gNodeExt,
              here->BSIM4grgeltd/T1);
    }
```

New Release

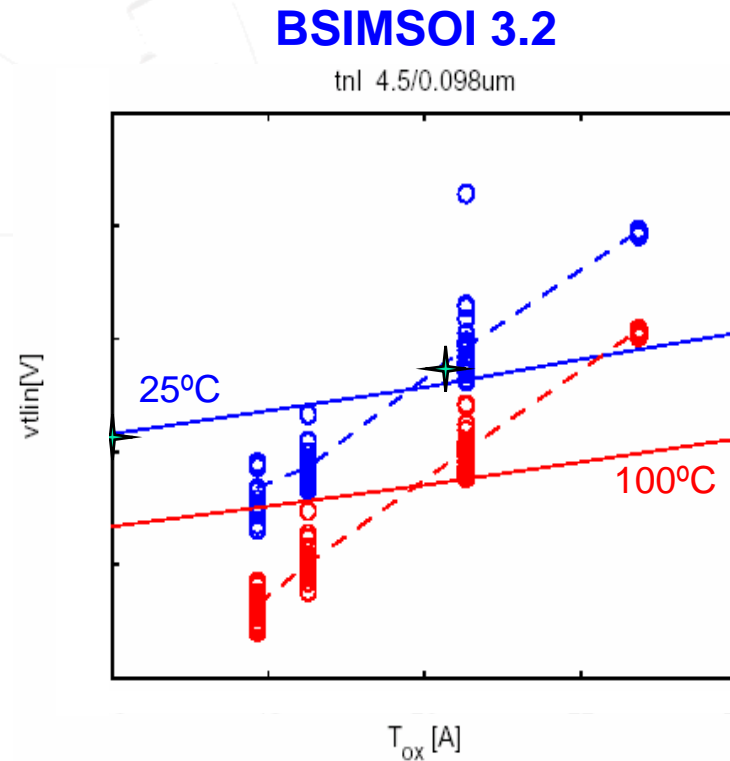
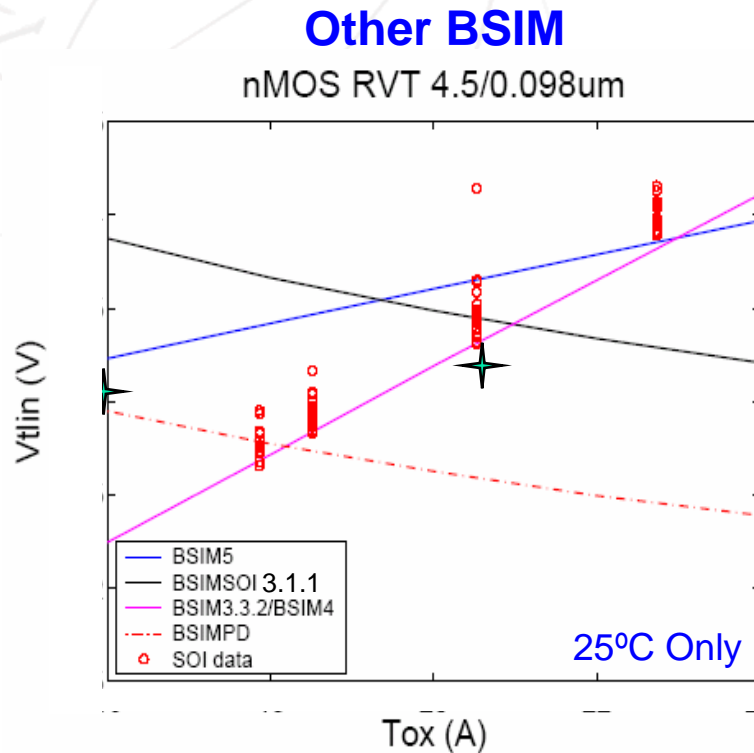
- **BSIM4.6.0 will be released soon with all the improvements/bug fixes after the asymmetric leakage model testing is finished. (TI and ADI are testing it)**



BSIMSOI Improvements

BSIMSOI3.2 Oxide Scalability Issue (I)

- BSIMSOI3.2 gives very weak T_{ox} dependence on threshold voltage.
 - Reported by **Judy An, AMD**



BSIMSOI3.2 Oxide Scalability Issue (II)

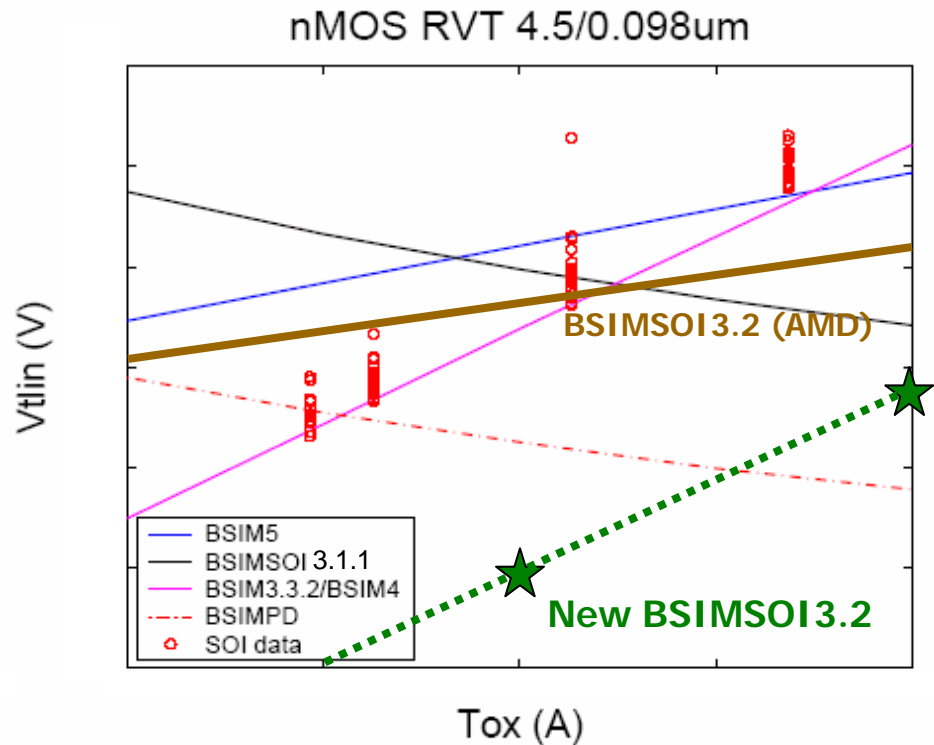
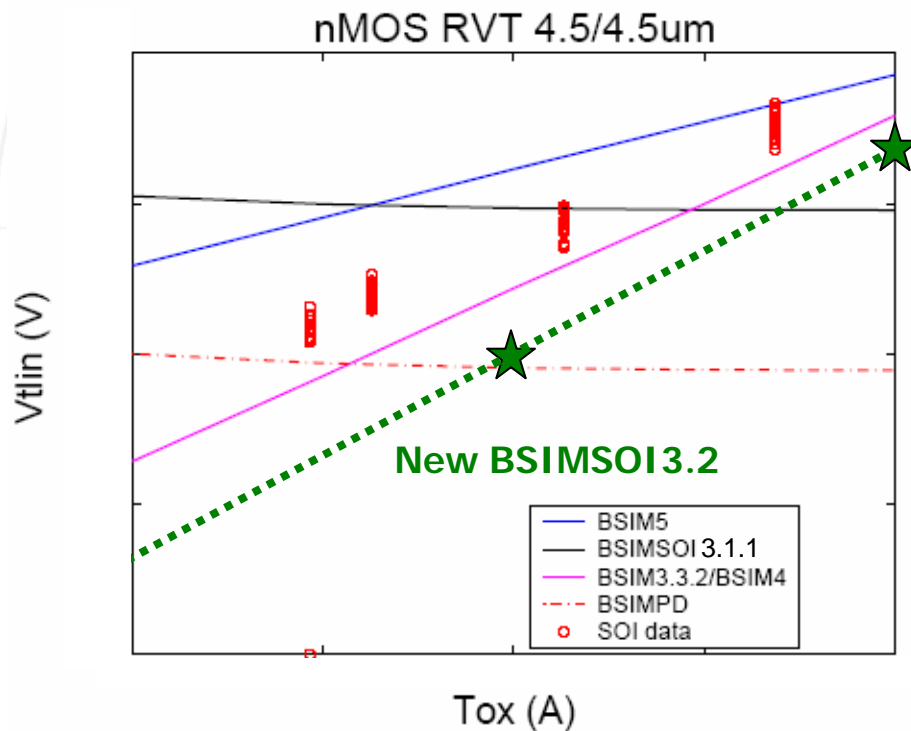
- **Bugs:** In BSIMSOI3.2, K_{1ox} ($=K_{1eff} * T_{ox}/T_{oxm}$) is added for oxide scalability. However, there are some places where we don't need tox dependence for K_{1eff}
- For example, in V_{th} calculation:

$$\begin{aligned}
 V_{th} = & V_{tho} + (K_{1ox} \text{sqrtPhisExt} - K_{1eff} \sqrt{\Phi_s}) \sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox} V_{bseff} \\
 & + K_{1ox} \left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K_3 + K_{3b} V_{bseff}) \frac{T_{ox}}{W_{eff}' + W_o} \Phi_s \\
 & - D_{VT0w} \left(\exp\left(-D_{VT1w} \frac{W_{eff}' L_{eff}}{2l_{nw}}\right) + 2 \exp\left(-D_{VT1w} \frac{W_{eff}' L_{eff}}{l_{nw}}\right) \right) (V_{bi} - \Phi_s) \\
 & - D_{VT0} \left(\exp\left(-D_{VT1} \frac{L_{eff}}{2l_i}\right) + 2 \exp\left(-D_{VT1} \frac{L_{eff}}{l_i}\right) \right) (V_{bi} - \Phi_s) \\
 & - \left(\exp\left(-D_{sub} \frac{L_{eff}}{2l_{to}}\right) + 2 \exp\left(-D_{sub} \frac{L_{eff}}{l_{to}}\right) \right) (E_{tao} + E_{tab} V_{bseff}) V_{ds} \\
 & - n v_t \cdot \ln \left(\frac{L_{eff}}{L_{eff} + DVTP0 \cdot (1 + e^{-DVTP1 V_{ds}})} \right)
 \end{aligned}$$

- **Action:** replace the K_{1ox} with K_{1eff} will resolve this issue

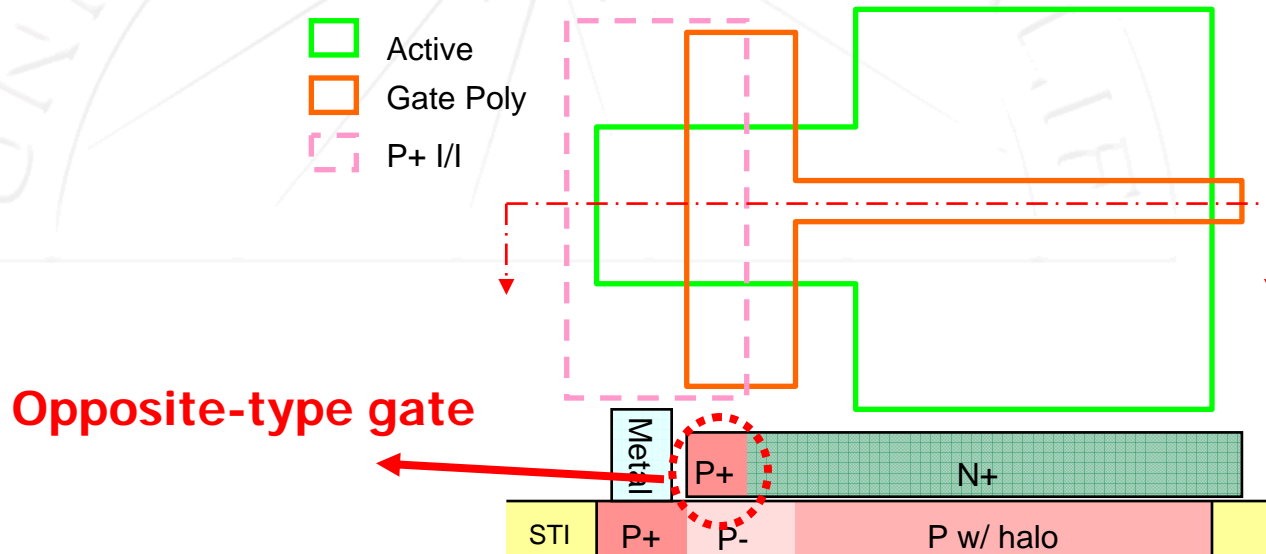
Model Verification

- Use BSIMSOI3.2 sample model card on BSIMSOI website
- V_{tlin} is extracted at $I_{ds} = (300 \text{ nA}) * (W/L) @ V_{ds} = 0.05V$
- Slope matches the Si data (absolute value can be modified by parameter extraction)



C-V Model Improvement

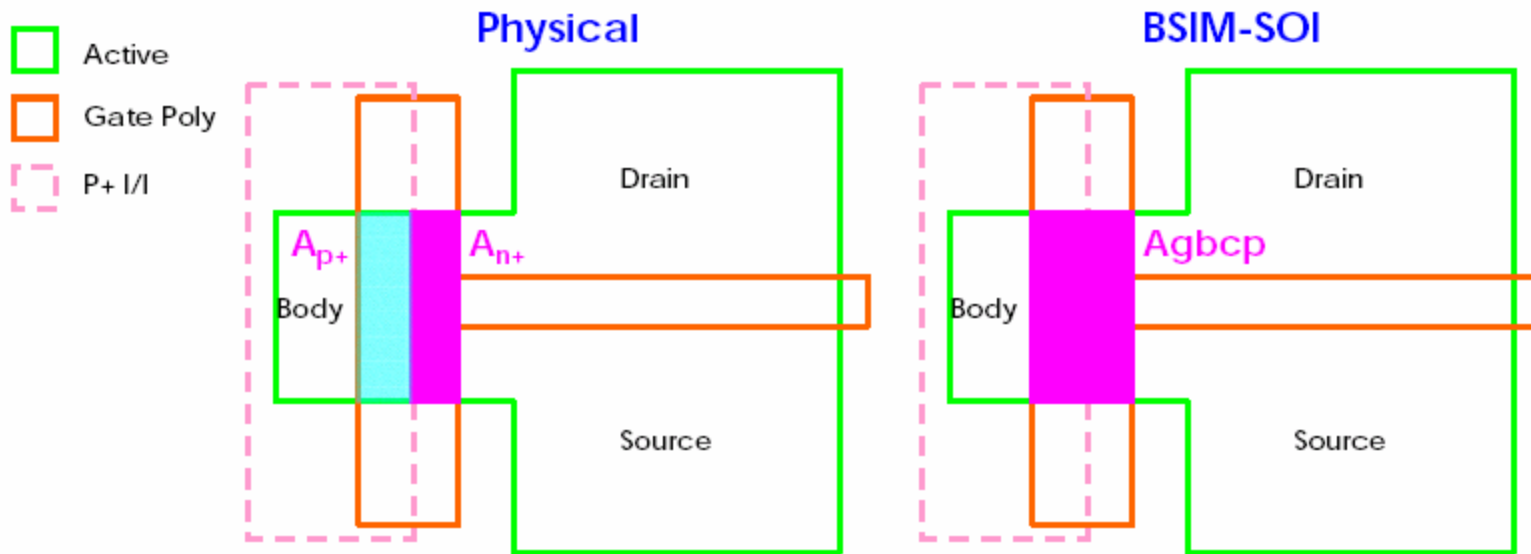
- Overestimation of gate charge in the body contact transistor due to opposite-type gate parasitic cap.
 - Reported by **Jung-Suk Goo, AMD**



Source: J.-S. Goo, MOS-AK 2005

- The P+ implantation for body contact will induce a parasitic P⁺-poly gate MOSCAP
- Charge on gate now consists of N⁺/P and P⁺/P⁻ MOS-CAP.

Current BSIMSOI Capacitance Model

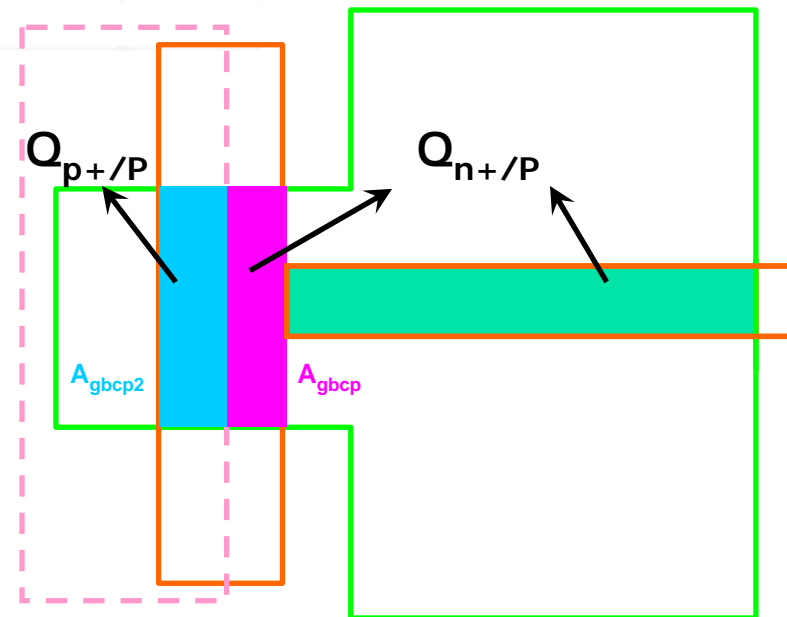


- In the current BSIMSOI model, the parasitic gate-to-body overlap due to body contact is modeled by one MOSCAP only (N+/P here)
- This leads to an overestimation of gate charge and hence larger delay in circuits.

Modified C-V Model

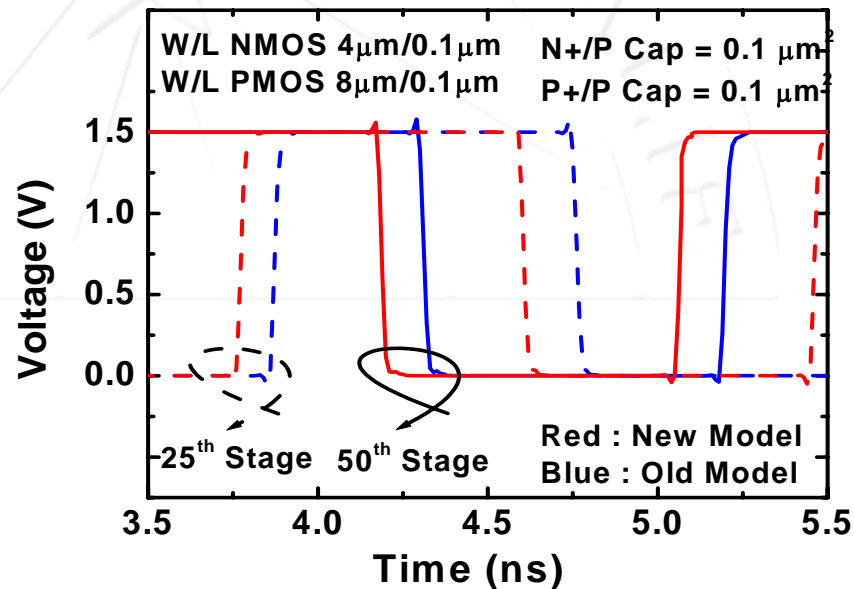
- Charge model modified to include the effect of p⁺/P region.
- Higher V_{FB} in the p⁺/P region lowers the gate charge and changes the C-V.
- Net gate charge is sum of n⁺/P region and p⁺/P region as shown below.
- One new model parameter **CR** to account for the non-ideal process variations
 - $A_{gbcp1} = A_{gbcp} * CR$
 - $A_{gbcp2} = A_{gbcp} * (1-CR)$

$$\begin{aligned}
 \text{Final charge} = & A_{gbcp1} \times n^+/\text{NMOS} \\
 & + WL \times n^+/\text{NMOS} \\
 & + A_{gbcp2} \times p^+/\text{NMOS}
 \end{aligned}$$



New Model Results

- 51- stage ring oscillator shows a smaller delay/stage (6%) due to lower capacitance.



- The accuracy of the SOI model for body contacted device has been enhanced.
- More testing is undergoing at Berkeley and AMD

BSIMSOI3.2 Requests

- Turn-on slope of C-V curve (@moderate inversion region) does not match the data
 - Reported by **Richard Williams, Cal Bittner, IBM**
 - Suggested solution: Make $V_{gsteffCV}$ in the C-V follow m^* implementation used in the I-V model

Original (v3.2) implementation

$$V_{gsteffCV} = n v_t \ln \left(1 + \exp \left[\frac{V_{gs} - V_{th}}{n v_t} \right] \cdot \exp \left[- \frac{delvt}{n v_t} \right] \right)$$

Introduce m^* implementation in the I-V V_{gsteff} (for accuracy improvement in the moderate inversion region)

Effective V_{gst} for all region (with Polysilicon Depletion Effect)

- Action: modify the $V_{gsteffCV}$ equation and test it

$$V_{gsteff} = \frac{n v_t \ln \left[1 + \exp \left(\frac{m^* (V_{gs_eff} - V_{th})}{n v_t} \right) \right]}{m^* + n C_{ox} \sqrt{\frac{2 \Phi_s}{q \epsilon_{si} N_{dep}}} \exp \left(- \frac{(1 - m^*) (V_{gs_eff} - V_{th}) - V_{off}}{n v_t} \right)}$$

BSIMSOI4.0 Requests

- **Igisl term is missing (which was present in V3.2), needed for asymmetric model**
- **Reported by Richard Williams, Cal Bittner, IBM**
 - Action: will put the Igisl back for the asymmetric model

- **Small value of Tcen will create NaNQ issue**
 - **Reported by Richard Williams, Cal Bittner, IBM**
 - Suggested solution: add clamp at line 4750 on Tcen in b4soild.c

```
+4750          Tcen = pParam->B4SOIIdcb - 0.5 * (V3 + V4);
+4751          T1 = 0.5 * (1.0 + V3 / V4);
+4752 // Tcen can underflow with right combination of tox, dtoxv, nch, bias
+4753          if (Tcen < 1e-15) {
+4754              Tcen = 1e-15;
+4755              T1 = 1e-6;
+4756          }
```

- Action: will test the suggested solution
- **Add all four charges to debug=1 outputs**
 - Action: will add qdrn, qsrc, qgate, qsub for debug=1 outputs

BSIMSOI4.0 Bug Reports

- **rdsmod = 1 (b4soild.c) – external resistors vs rdsw**

- Reported by **Richard Williams, Cal Bittner, IBM**

- **Bug:**

```
+4138      T4 = pParam->B4SOIrd0 * 0.5;  
+4139      Rd = pParam->B4SOIrdwmin + T3 * T4;
```

last two lines should be:

```
+4138      T4 = rd0 * 0.5;  
+4139      Rd = rdwmin + T3 * T4;
```

- **Action:** change b4soild.c accordingly

- **Vt equation for soiMod = 1,2 – FD subthreshold slope term**

- Reported by **Richard Williams, Cal Bittner, IBM**

- **Bug:**

```
+1422      T3 = pParam->B4SOIcdsc + pParam->B4SOIcdscb * Vbseff  
+1423      + pParam->B4SOIcdscd * Vds;
```

Vbseff should be replaced by Vbs0mos

```
+1422      T3 = pParam->B4SOIcdsc + pParam->B4SOIcdscb * Vbs0mos  
+1423      + pParam->B4SOIcdscd * Vds;
```

- **Action:** change b4soild.c accordingly

BSIMMG 1.0 alpha Release

- BSIMMG1.0 alpha version has been released for modeling multi-gate transistor
- BSIMMG1.0 alpha version has the following features:
 - A surface-potential-based model with surface potential solved analytically
 - Important second order effects, such as body doping effect, short channel effect, drain-induced-barrier lowering, mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, poly depletion, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance models, are incorporated in the model.
 - BSIMMG is released in Verilog-A.
- If you are interested in conducting this alpha version test and agree to promptly send us bug reports and suggestions, please email Chung-Hsun Lin (chl@eecs.berkeley.edu) with the subject "BSIMMG1.0 alpha version code request".

Acknowledgement

- BSIM team would like to thank Claude Cirba (TI), David Zweidinger (TI), Yong Liu (TI), Keith Green (TI), Geoffery Coram (ADI), Richard Williams (IBM), Cal Bittner (IBM), Josef Watts (IBM), Judy An (AMD), Jung-Suk Goo (AMD), Qiang Chen (AMD), Weidong Liu (Synopsys), Jane Xi (Intel) for the invaluable discussions and help with simulations
- New Postdoc, Morgan Yang, will arrive at Berkeley in late Oct. for supporting BSIM research.



Suggestions / Feedback?