

HiSIM Present Status

HiSIM Team

**Presenter: Prof. Tatsuya Ezaki
(CMC Meeting in Raleigh, 30. June, 2005)**

Release Actions Done

28th May: release test

30th May: release start

- **Source Code (C-Code)**
- **Manual**
- **Parameter-Extraction Procedure**

Version-up Plan

15th July: bugfix and Verilog-A code after request

15th August: bugfix and version-up

15th September: if necessary

Support System

Mailing list:

ml-hisim-cmc@hiroshima-u.ac.jp (CMC members)

used for possible announcement

ml-hisim-tech@hiroshima-u.ac.jp (HU members)

for technical questions such as:

- parameter extraction
- circuit convergence
- model deficit
- bugs

ml-hisim-admin@hiroshimau-u.ac.jp (HU members)

for administrative questions such as:

- NDA matters
- requests for future functionality
- general questions

Up-To-Date Information

Please visit our website:

<http://www.hiroshima-u.ac.jp>

New HiSIM Support Organization

- **HiSIM Center at Hiroshima University**
- **Temporary HiSIM Office in San Francisco**

About the Source-Code Released in May

- **I(gate) and I(diode) models cause convergence problems with SPICE3f5 for some circuits.
Please wait for the 15th July release, where these problems will be fixed, with your testing of I(gate) and I(diode) models.**
- **A further bug causing convergence problems for positive source-bulk voltage has been found. These convergence problems can be removed by setting model parameter BS1 to zero. Instruction for fixing this bug in the source code were published on our website on 20th June together with another bug.**
- **Genetic Algorithm soft ware for parameter extraction will be available for CMC members in August.
It is presently going through a final test procedure.**