

CMC LDMOS standardization

CMC LDMOS subcommittee

Goal:

To seek for an existing LDMOS compact model (not a sub-circuit based one) developed for circuit simulation, after evaluation, select the best to be the CMC standard LDMOS model. Support and regulate the future development and release of this LDMOS model according to the requirements of CMC.

Schedule for LDMOS Standardization:

Stage 1: Preparation

1. By email among CMC LDMOS subcommittee, Collect and discuss requirements for a LDMOS model as a standard CMC model and come up a proposal by end of Feb. 2006. Collect possible candidates at the same time.
2. LDMOS sub-committee meeting in the evening before March 10th CMC meeting in 2006, face to face discussion the details of the proposal, and try to finalize it on the CMC meeting the day after or in a short of time after the CMC meeting
3. Post the finalized requirement on CMC web, and actively contact the developers for possible candidates, and come up a list of candidates before the next CMC meeting in May 2006.

Stage 2: Evaluation

1. Depends on how many candidates we have, we will discuss the evaluation plan and refine the requirement as needed in May 2006 CMC meeting. In this meeting, we will invite the developers for possible standard LDMOS model candidates for discussion.
2. Sets of LDMOS measurement data covering DC, AC, Noise and RF measurement are solicited to be used during model evaluation. Ideally, the data set can cover the bias, temperature range specified in the requirement list.
3. Give a certain time of period determined in the evaluation plan, say two quarters, to the developers for them to prepare the report.
4. During this time, a beta version is required for interested CMC members to do in-house testing. Volunteers within CMC LDMOS subcommittee are invited to carry out the LDMOS model evaluation. Model developers are required to provide feasible way for CMC members to do the evaluation. Say, providing either C-code in Spice3 interface, or Verilog-A code or providing free license of model validation tools if using internal format for model implementation.
5. Then in a later CMC meeting (Say, December 2006), developers report their model evaluation results. CMC members/Volunteers report their evaluation results.
6. A voting will be done either in the meeting or after the meeting to select the candidate if needed.

Stage 3: Release of formal version as CMC standard LDMOS model and ongoing development

1. LDMOS sub-committee will act as interface between CMC members and the developer to ensure the selected LDMOS model development and release are aligned with CMC requirements
2. The release of LDMOS standard model will follow the CMC standard model release procedure

Standard LDMOS requirements:

Considerations in must-have and nice-to-have item lists:

1. Put only critical requirements for a general LDMOS model in the must-have items list, since those must-have items are minimal requirements for the standard CMC LDMOS model
2. The requirements are more target-oriented rather than modeling approaches and specific features of LDMOS.
3. Requirements for an LDMOS model follow the general requirements that have been set by CMC including code requirement and release procedure.

Must-have model features:

1. Capable for analog and RF IC simulations, which requires
 - a. Accurate modeling of DC/AC behavior as well as the derivatives of terminal currents and node charges with respect to node voltages for all working modes (off, linear, saturation regions and reverse modes). Charge model has to be charge conservative, and intrinsic charge model has to take into account the effects of voltage drop across the source and drain resistances.
 - b. Accurate modeling of drain extension (drift region) region resistance including velocity saturation.
 - c. Accurate modeling of gate/drain overlap region bias dependent capacitance and resistance.
 - d. Accurate modeling of parasitic effects (gate, source and drain, and substrate resistances, and source/drain-body junction diodes)
 - e. Accurate modeling of the 1/f, thermal, and gate induced noise.
2. Capable of modeling accurately with power supplies up to 200 volts and temperature ranges from -50°C to 200°C .
3. Capable of modeling self-heating effects accurately and efficiently, which requires scalable temperature-dependence modeling.
4. Capable of modeling accurately quasi-saturation effects and G_m fall-off in the saturation region, namely, the channel current compressions at higher V_{gs} when V_{ds} is greater than V_{dsat} .
5. Capable of modeling accurately Cgd drop at higher external V_{gs} biases.

6. Capable of accurate modeling of the true asymmetry of the source and drain resistances and the source and drain junctions in IV and CV.
7. Capable of modeling substrate current behavior correctly including the impact ionization taking place in the drain drift extension regions.
8. Capable of handling scalability over a wide range of geometries, biases, and temperatures with one set of global model parameter set to cover the entire device matrix provided for model extraction. Provides drain drift region length as an instance parameter.
9. Capable of covering reverse working mode for both symmetric and asymmetric structure (i.e. when $V_{ds} < 0$)
10. Capable of handling of p-type devices as well as n-type devices.
11. Capable of prediction correctly breakdown behavior.
12. Good convergence in reasonable scale circuit simulation.

Nice-to-have model features:

1. Capable of modeling accurately a wide array of HV-MOSFET process technologies and device structures, which would include LDMOS and EDMOS (Extended Drain), both symmetrical and asymmetrical, and other drain drift extension structures including, but not limited to, those of various RESURF flavors.
2. Capable of modeling accurately the long-channel DIBL and R_{out} degradation for drain extended devices.
3. Capable of modeling layout dependent characteristics including multi-finger device structures that have separate, merged, and shared source and drain connections, and point and wide source/drain contacts.
4. Capable of modeling body bias dependency of DC and AC characteristics, as well as V_{ds} -dependence of the body bias effects.
5. Capable of modeling multiple junctions for complicated LDMOS drain structures.
6. Capable of providing optional temperature node for thermal electrical coupling simulation.
7. Capable of accurately modeling the non-quasi-static effects up to 20GHz.
8. Capable of creating accurate statistical models
9. Capable of modeling diode breakdown.
10. Capable of modeling parasitic BJT effects.
11. Capable of modeling gate current due to hot carrier in channel and tunneling
12. Capable of handling body diode model reverse recovery and high-level current injection effect
13. Capable of handling second breakdown characteristics
14. Capable of identification of SOA violations
15. Capable of handling thermal run away

Supporting requirement:

1. Agree to open source code and model document including detailed model equations to public once the model is selected to CMC standard LDMOS model.

2. Provide documented example and working model parameter extraction flows and strategies.
3. Provide an infrastructure with equal and timely access to all the information and materials regarding the model itself and model version updates and releases available to all interested CMC member companies. Must follow the CMC standard model QA and release processes and guidelines.
4. Provide a working and efficient mechanism for technical supports.