

# HICUM/Level2 - Update

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## Availability of HICUM in Circuit Simulators

(version numbers and some comments refer to latest tests (dated 6/04) at STM on LNA, mixer and frequency divider)

(Please contact simulator vendor or see vendor web-site for details and the latest status of availability)

<i>simulator</i>	<i>1<sup>st</sup> release</i>	<i>latest version</i>	<i>L2-V</i>	<i>L0-V</i>	<i>comments</i>
<b>ADS</b>	<b>7/00</b>	<b>ADS2003C</b>	2.1	1.0	very stable and fast; received version 1.1
<b>ELDO-RF</b>	<b>10/99</b>	<b>AMS2004.1/2</b>	2.1	rec 1.1	very stable and reasonably fast
<b>AnalogOffice</b>	<b>2003</b>	<b>rel. 04/04</b>	2.1	1.0	numerically stable
<b>SPECTRE-RF</b>	<b>10/99</b>	<b>5.0.33.031104</b>	2.1	rec 1.1	have now promised to fix bugs in L2
<b>Smart-SPICE</b>	<b>11/00</b>	<b>rel. 11/00</b>	2.?		can be combined with UTMOST
<b>APLAC</b>	<b>10/01</b>	<b>7.92c</b>	2.1	rec 1.1	still limited stability for L2
<b>HSPICE</b>	<b>2/01</b>	<b>2004.2-beta2</b>	2.1	rec 1.1	full compatibility with AWR-AO for L2
<b>TEKSPICE</b>	<b>8/02</b>	<b>rel. 8/02</b>	2.?		proprietary numerical improvements for L2
<b>GoldenGate</b>	<b>?/03</b>	<b>3.3.14</b>	2.?		
<b>HSIM</b>	<b>4/02</b>	<b>5.0_2004.20.7</b>	2.?		
<b>SPICE3F5</b>	<b>4/02</b>	<b>11/04</b>	rec 2.2	rec 1.1	reference simulator with HB capability

- Various other (partially in-house) simulators (ASX (IBM), Eagleware, Micro-Cap, NEXXIM (Ansoft) ...)
- Verilog-A version of model code; also, stand-alone kit enabling coupling with other tools

# HICUM/Level2 - Update

- **Version 2.1**
  - supporting model deployment and simulator implementation
    - see separate slide on latest status of availability
  - Cadence has promised to fix bugs, but no feedback yet from Cadence/users regarding completion
    - => reliable SPECTRE implementation prior to version 2.2. release will be useful
- **Version 2.2**
  - thorough testing of simulator implementation in parallel at CEDIC (since mid October) and ST, CAEN (recently started)
  - Verilog-A implementation has started
  - new DEVICE version has been released to cooperation partners for testing V2.2
  - delay (testing, documentation) due to unexpected high demand for HICUM/Level0

# HICUM/Level0 - Update

- Version 1.1
  - fairly high demand recently => requested by all major simulator vendors
  - implementation status see separate slide "Simulator Availability" (now also includes Level0 update)
  - updated version 1.1 has been created that incorporates some of the HICUM/Level2 improvements (e.g., hyperbolic smoothing, improved temperature description)
  - Verilog implementation ongoing
  - presently working on model verification for different process technologies and generations (with  $f_T$  ranging from 50GHz to over 200GHz) from several companies, such as Atmel, Infineon, Jazz, ST

Note: this model has been requested by CMC members, but is presently not financially supported by the CMC